Manual Change

Agilent Part No. 16000-99026

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Change

Change the company name from (YOKOGAWA-) HEWLETT-PACKARD, LTD., or its abbreviation HP (YHP) to Agilent Technologies or Agilent.

This document may contain references to HP (YHP) or (Yokogawa-) Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. To reduce potential confusion, the only change to product numbers and names has been in the company name prefix: where a product number/name was HP XXXX the current name/number is now Agilent XXXX. For example, model number HP4294A is now model number Agilent 4294A.

マニュアル・チェンジ

変更

本文中の「HP(YHP)」、または「(横河)ヒューレット・パッカード株式会社」という語句を、「Agilent」、または「アジレント・テクノロジー株式会社」と変更してください。

ヒューレット・パッカード社の電子計測、半導体製品、化学分析ビジネス部門は分離独立し、アジレント・テクノロジー社となりました。
社名変更に伴うお客様の混乱を避けるため、製品番号の接頭部のみ変更しております。
（例：旧製品名　HP 4294A　は、現在　Agilent 4294A　として販売いたしております。）

HP 4286A RF LCR Meter

Service Manual

SERIAL NUMBERS

This manual applies directly to instruments with serial number prefix JP1KC. For additional important information about serial numbers, read "INSTRUMENT COVERED BY THIS MANUAL" in General Information of this service manual.

HP Part No. 04286-90111
Printed in JAPAN April 1999

Notice

The information contained in this document is subject to change without notice.

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Manual Printing History

The manual printing date and part number indicate its current edition. The printing date changes when a new edition is printed. (Minor corrections and updates that are incorporated at reprint do not cause the date to change.) The manual part number changes when extensive technical changes are incorporated.

July 1995 ..... First Edition

April 1999 ..... Second Edition

Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific *WARNINGS* elsewhere in this manual may impair the protection provided by the equipment. In addition it violates safety standards of design, manufacture, and intended use of the instrument.
The Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

Note 

HP 4286A is designed for use in INSTALLATION CATEGORY II according to IEC 61010-1 and POLLUTION DEGREE 1 according to IEC 61010-1 and IEC 60664-1. HP 4286A is an INDOOR USE product.

Note 

LEDs in HP 4286A are Class 1 in accordance with IEC60825-1.
CLASS 1 LED PRODUCT

Ground The Instrument

To avoid electric shock hazard, the instrument chassis and cabinet must be connected to a safety earth ground by the supplied power cable with earth blade.

DO NOT Operate In An Explosive Atmosphere

Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

Keep Away From Live Circuits

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with the power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT Service Or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT Substitute Parts Or Modify Instrument

Because of the danger of introducing additional hazards, do not install substitute parts or perform unauthorized modifications to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings , such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

Warning

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting this instrument.

Typeface Conventions

Bold	Boldface type is used when a term is defined. For example: **icons** are symbols.
Italics	Italic type is used for emphasis and for titles of manuals and other publications. Italic type is also used for keyboard entries when a name or a variable must be typed in place of the words in italics. For example: `copy` *filename* means to type the word `copy`, to type a space, and then to type the name of a file such as `file1`.
`Computer`	Computer font is used for on-screen prompts and messages.
HARDKEYS	Labeled keys on the instrument front panel are enclosed in ▢.
SOFTKEYS	Softkeys located to the right of the CRT are enclosed in ▯.

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology, to the extent allowed by the Institution's calibration facility, or to the calibration facilities of other International Standards Organization members.

Warranty

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from the date of shipment, except that in the case of certain components listed in *General Information* of this manual, the warranty shall be for the specified period. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instruction when property installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

Limitation Of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

No other warranty is expressed or implied. HP specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

Exclusive Remedies

The remedies provided herein are buyer's sole and exclusive remedies. HP shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract, tort, or any other legal theory.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

Safety Symbols

General definitions of safety symbols used on equipment or in manuals are listed below.

Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual.

Alternating current.

Direct current.

On (Supply).

Off (Supply).

Warning

This **Warning** sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

Caution

This **Caution** sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

Note

Note denotes important information. It calls attention to a procedure, practice, condition or the like, which is essential to highlight.

Documentation Map

The following manuals are available for the HP 4286A:

- **Operating Manual Set (HP Part Number 04286-90030)**

  The *Function Reference* describes all functions accessed from the front panel keys and softkeys. It also provides the HP 4286A features, specifications, information on options and accessories available.

- **Users Guide (HP Part Number 04286-90031)**

  The *Users Guide* walks you through system setup and initial power-on, shows how to make basic measurements, explains commonly used features, and typical application measurement examples. After you receive your HP 4286A, begin with this manual.

- **Programming Manual (HP Part Number 04286-90027)**

  The *Programming Manual* provides how to write BASIC program to control the HP 4286A using HP-IB, and a summary of all available HP-IB commands.

- **HP Instrument BASIC Users Handbook (Option 1C2 only), (HP Part Number E2083-90000)**

  The *HP Instrument BASIC Users Handbook* introduces you to the HP Instrument BASIC programming language, provides some helpful hints on getting the most use from it, and provides a general programming reference. It is divided into three books, *HP Instrument BASIC Programming Techniques* , *HP Instrument BASIC Interface Techniques* , and *HP Instrument BASIC Language Reference*.

- **HP Instrument BASIC Users Handbook Supplement (Option 1C2 Only), (HP Part Number 04286-90005)**

  The *HP Instrument BASIC Users Handbook Supplement* describes how HP Instrument BASIC works with the HP 4286A.

- **Service Manual (Option 0BW only), (HP Part Number 04286-90111)**

  The *Service Manual* explains how to do performance tests, and to adjust, troubleshoot, and repair the instrument.

Contents

3. Adjustments and Correction Constants

4. Overall Troubleshooting

Figures

Tables

1

General Information

INTRODUCTION

This *Service Manual* is a guide to servicing the HP 4286A RF LCR Meter. This manual contains information about performance testing, adjusting, troubleshooting, and repairing the HP 4286A.

ORGANIZATION OF SERVICE MANUAL

This manual consists of major chapters listed below. This section describes the names of the tabs and the content of each chapter.

- *Performance Tests* provides procedures for performance testing the HP 4286A.
- *Adjustments and Correction Constants* provides procedures for adjusting the HP 4286A after repair or replacement of an assembly. In the OSC level adjustment, the correction constants stored in the EEPROM on the A1 CPU are updated. The correction constants are updated by using the adjustment program (PN 04286-65002).

Note The next six chapters are the core troubleshooting chapters.

- *Overall Troubleshooting.* outlines the HP 4286A troubleshooting, and provides troubleshooting procedures to isolate the faulty functional group. Faulty assembly isolation procedures for each functional group follow this chapter.
- *Power Supply Troubleshooting*
- *Digital Control Troubleshooting*
- *Source Troubleshooting*
- *Receiver Troubleshooting*
- *Test Head Troubleshooting*

Note The following chapters are, for the most part, reference material.

- *Service Key Menus* documents the functions of the menus accessed from (System), SERVICE MENU. These menus let the operator test, verify, adjust, control, and troubleshoot the HP 4286A. HP-IB service mnemonics are included.
- *Theory of Operation* explains the overall operation of the HP 4286A, the division into functional groups, and the operation of each functional group.

- *Replaceable Parts* provides part numbers and illustrations of the replaceable assemblies and miscellaneous chassis parts, together with ordering information.
- *Replacement Procedures* provides procedures to disassemble portions of the HP 4286A when certain assemblies are to be replaced.
- *Post-Repair Procedures* contains the table of related service procedures. It is a table of adjustments and verification procedures to be performed after repair or replacement of each assembly.
- *Appendices* contains the manual changes information (required to make this manual compatible with earlier shipment configurations of the HP 4286A), and the power requirement.
- *Messages* contains the service related error message list.

INSTRUMENT COVERED BY MANUAL

Hewlett-Packard uses a two-part, ten-character serial number that is stamped on the serial number plate (see Figure 1-1) attached to the rear panel. The first five digits are the serial prefix and the last five digits are the suffix. The same prefix is used for all identical instruments. The prefix changes only when a change is made to the instrument. However, the suffix is assigned sequentially and is unique to each instrument. The contents of this manual apply to instruments with the serial number prefixes listed under **SERIAL NUMBERS** on the title page.

Figure 1-1. Serial Number Plate

An instrument manufactured after the printing date of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates that the instrument is different from those described in this manual. The manual for an unlisted instrument may be accompanied by a yellow *Manual Changes* supplement or have a different manual part number. The *Manual Changes* supplement contains "change information" that explains how to adapt the manual to newer instruments.

In additions to change information, the supplement may contain information for correcting errors (Errata) in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest *Manual Changes* supplement. The supplement for this manual is identified by this manual's printing data and is available from Hewlett-Packard. If the serial prefix or number of an instrument is lower than that on the title page of this manual, see *Appendix A, Manual Changes*.

For information concerning serial number prefixes not listed on the title page or in the *Manual Changes* supplement, contact the nearest Hewlett-Packard office.

TABLE OF SERVICE TEST EQUIPMENT

The first part of Table 1-1 lists all of the equipment required to performance test, adjust, and troubleshoot the HP 4286A. The table also notes the use and critical specifications of each item, and the recommended models. Equipment other than the recommended models may be substituted if the equipment meets or exceeds the critical specifications.

In addition to test equipment listed in Table 1-1, the following tools are also required:

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small)
- Pozidriv screwdriver, pt size #2 (medium)
- IC extractor
- Open-end wrench, 1/4 inch
- Open-end wrench, 5/16 inch
- Torque wrench, 3/4 inch, 136 N-cm
- Hex socket, 7/32 inch (5.5 mm)
- Flat edge screwdriver

Table 1-1. Recommended Test Equipment

Equipment	Critical Specifications	Recommended Model/ HP Part Number	Qty	Use[1]
Computer	HP 9000 Series 200/300[2]		1	A
BASIC Operating System	Revision 5.0 or above		1	A
Mass Storage	3.5 inch Microfloppy Disk Drive		1	A
Program	HP 4286A Adjustments Program (3.5 inch)	PN 04286-65002	1	A
Performance Test Kit	No substitute	HP 16190A	1	P
APC7 Calibration Kit[3]	No substitute	HP 16195A	1	P, T
Frequency Counter	Frequency Range: 20 MHz to 1 GHz, Time Base Error: $\leq \pm 1.9 \times 10^{-7}$/year	HP 5343A Opt. 001	1	P, A
Spectrum Analyzer	Frequency Range: 100 kHz to 4 GHz	HP 8566A/B	1	A, T
Power Meter	No substitute	HP 436A Opt. 022, HP 437B, or HP 438A	1	P, A
Power Sensor	Frequency Range: 20 MHz to 1.8 GHz, Power: +5 dBm to −20 dBm	HP 8482A	1	P, A
Oscilloscope	Band width $\geq$ 100 MHz	HP 54111D	1	T
Oscilloscope Probe	Impedance: 1 MΩ	HP 10431A	1	T
Handler Simulator	No substitute	04278-65001	1	T

1 P: Performance Tests, A: Adjustments and Correction Constants, T: Troubleshooting

2 Excluding HP 9826A

3 Required for testing the HP 4286A of option 001 which does not furnish the APC7 calibration kit.

Table 1-1. Recommended Test Equipment (continued)

Equipment	Critical Specifications	Recommended Model/ HP Part Number	Qty	Use[1]
Cables, Adapters	Type-N cable, 50 Ω	HP 11500B or part of HP 11851B[1]	1	A, T
	BNC cable, 61 cm, 50 Ω	PN 8120-1839	3	P, A, T
	BNC cable, 122 cm, 50 Ω	PN 8120-1840	2	P, A, T
	HP-IB cable	HP 10833A/B/C	3	A
	BNC(f)-SMA(f) adapter, 50 Ω	PN 1250-0562	1	P, A
	SMC(f)-BNC(f) adapter, 50 Ω	PN 1250-0832	1	A
	SMB(f)-BNC(f) adapter, 50 Ω	PN 1250-1236	1	A
	N(m)-BNC(f) adapter, 50 Ω	PN 1250-1476	2	P, A, T
	SMA(m)-BNC(f) adapter, 50 Ω	PN 1250-1548	1	T
	SMA(m)-SMA(f) right angle adapter, 50 Ω	PN 1250-1741	1	T
	APC3.5(m)-APC3.5(f) adapter, 50 Ω	PN 1250-1866	1	P, A
	APC7-N(f) adapter, 50 Ω	HP 11524A or part of HP 85032B[2]	1	P, A, T
	BNC(f)-SMA(m) adapter, 50 Ω	PN 1250-1548	1	A
	APC3.5(m)-APC7 adapter, 50 Ω	PN 1250-1746[3]	1	P, A, T
	APC3.5(m)-APC3.5(f) right angle adapter, 50 Ω	PN 1250-1249[4]	1	P, A, T
	Test fixture stand	PN 04286-60141[3]	1	P, A, T

1 The HP 11851B includes three N(m)-N(m) cables of 61 cm and a N(m)-N(m) cable of 88 cm.

2 The HP 85032B includes two APC7-N(f) adapters.

3 HP 4286A furnished accessory

4 HP 4286A option 021/022 furnished accessory

2

Performance Tests

INTRODUCTION

This chapter provides the HP 4286A RF LCR Meter performance tests information. These performance tests are used to verify that the HP 4286A's performance meets its specifications.

General information about the performance tests is provided first. Then, step by step procedures for each test are provided.

Each test procedure consists of the following parts:

Description:	describes the test procedure.
Test Equipment:	describes test equipment required in the test.
Procedure:	describes the test procedure step by step.

GENERAL INFORMATION

This section provides general information about the performance tests.

Warm Up Time

Allow the HP 4286A to warm up for at least 30 minutes before you execute any of the performance tests.

Ambient Conditions

Perform all performance tests in an ambient conditions of 23 ± 5°C, ≤ 70%RH.

Calibration Cycle

The HP 4286A requires periodic performance verification to remain in calibration. The frequency of performance verification depends on the operating and environmental conditions under which the HP 4286A is used. Verify the HP 4286A's performance at least once a year using the performance tests given in this chapter.

Performance Test Record

The performance test record lists all test points, acceptable test limits, test result entry columns, and measurement uncertainties. The measurement uncertainty shows how accurately the HP 4286A's specifications are measured and depends on the test equipment used. The listed measurement uncertainties are valid only when the recommended test equipment is used.

The performance test record is provided at the end of this chapter. Use the record as a master, and make extra copies for performance testing.

Recommended Test Equipment

Table 1-1 lists the equipment required for performance testing the HP 4286A. Other equipment may be substituted if the equipment meets or exceeds the critical specifications given in Table 1-1.

FREQUENCY ACCURACY TEST

Description

This test uses a frequency counter to measure the actual frequency of the HP 4286A test signal when it is set to 1 GHz.

Test Equipment

Frequency Counter	HP 5343A
BNC cable, 61 cm	PN 8120-1839
APC3.5(m)-APC3.5(f) adapter[1]	PN 1250-1866
N(m)-BNC(f) adapter	PN 1250-1476
BNC(f)-SMA(f) adapter	PN 1250-0562

[1]: This adapter is used to protect the HP 5343A's APC 3.5 Input connector, (it is sometimes called a "connector saver.") In the test setup, the BNC(m)-SMA(f) adapter is connected to the HP 5343A's APC 3.5 Input connector through this adapter. For more information on microwave connectors and connector care, see *MICROWAVE CONNECTOR CARE* (PN 08510-90064).

Procedure

1. Connect the test equipment as shown in Figure 2-1.

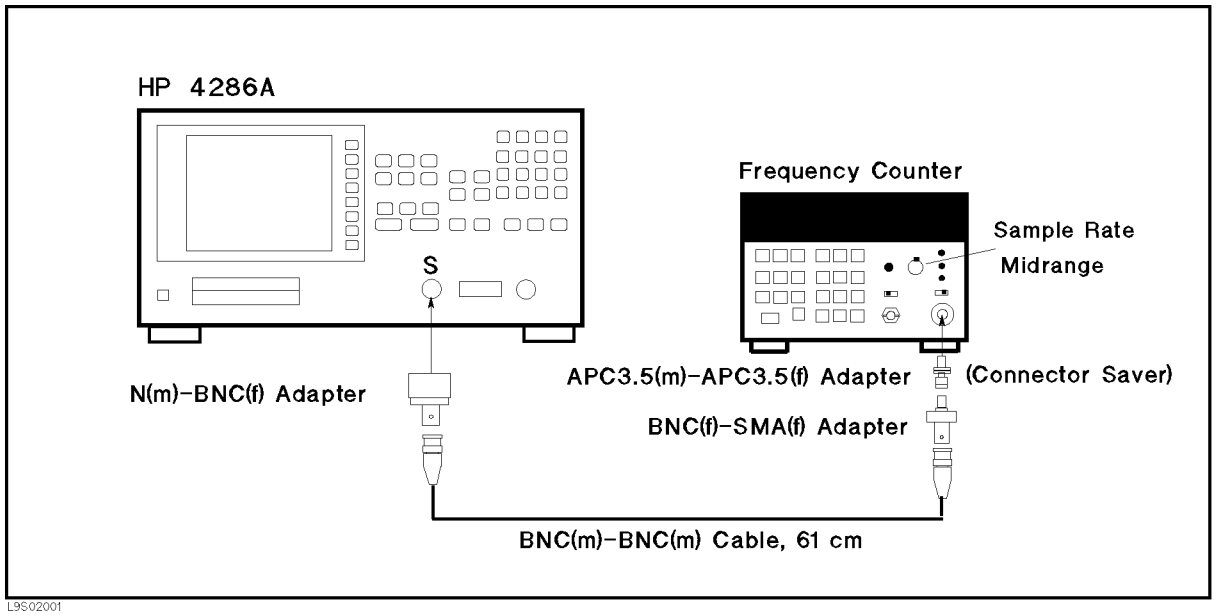


Figure 2-1. Frequency Accuracy Test Setup

Note

An APC3.5(m)-APC3.5(f) adapter is used between the BNC(f)-SMA(f) adapter and the HP 5343A's APC 3.5 Input connector to protect the HP 5343A's APC 3.5 Input connector. In Figure 2-1, the SMA connector of the BNC(f)-SMA(f) adapter is mated with the APC 3.5 connector of the "connector saver" adapter.

2. Initialize the frequency counter. Then set the controls as follows:

Controls	Settings
Sample Rate	Midrange
Range Switch	500 MHz-26.5 MHz
INT/EXT Switch (rear panel)	Internal

3. Press [Preset] to initialize the HP 4286A. Then set the controls as follows:

Control Settings	Keystrokes
Frequency: 1 GHz	[Sweep Setup], CLEAR LIST, YES, ADD, FREQ, [1], [G/n], SEGMENT DONE, LIST DONE
OSC Level: 0.2 V	[Source], [.], [2], [x1]

4. Wait for the frequency counter reading to settle.
5. Subtract 1 GHz (HP 4286A setting) from the frequency counter reading, and record the result on the performance test record.

OSC LEVEL ACCURACY TEST

Description

This test uses a power meter and a power sensor to measure the actual power level of the test signal at several frequency points. In the case of the 1 m test head (standard/option 021), the test frequency range is from 1 MHz to 1 GHz. In the case of 3 m test head (option 022/032), the test frequency range is from 1 MHz to 500 MHz.

Test Equipment

Power Meter	HP 436A Opt. 022, HP 437B, or HP 438A
Power Sensor	HP 8482A
APC7-N(f) Adapter	HP 11524A
APC3.5(m)-APC7 Adapter	PN 1250-1746[1]
APC3.5(m)-APC3.5(f) Right Angle Adapter	PN 1250-1249[2]
Test Fixture Stand	PN 04286-60141[1]

[1]: HP 4286A furnished accessory
[2]: HP 4286A option 021/022 furnished accessory

Procedure

1. Connect the power sensor to the power meter. Calibrate the power meter for the power sensor.
2. Connect the test head to the main frame, and set the test head on the test fixture stand. Then connect the APC3.5(m)-APC7 adapter to the test head. In the case of option 021/022 (Straight Angle Test Head), use the APC3.5(m)-APC3.5(f) right angle adapter to connect the APC3.5(m)-APC7 adapter to the test head.
3. Connect the power sensor to the test head as shown in Figure 2-2.

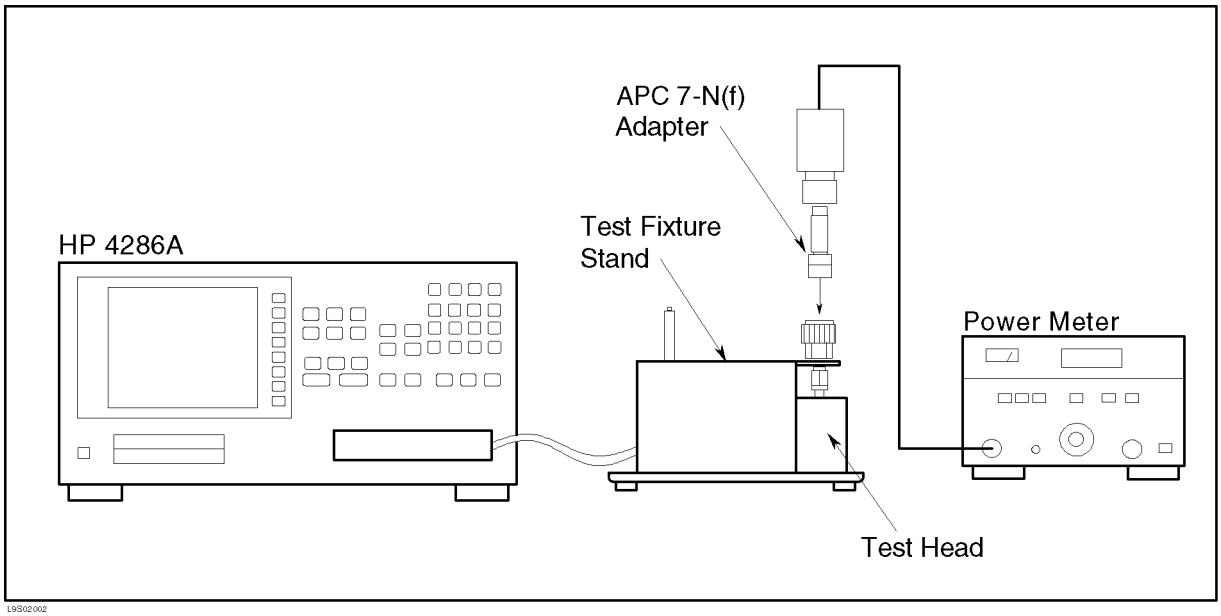


Figure 2-2. OSC Level Accuracy Test Setup

4. Press (Preset) to initialize the HP 4286A.
5. Press (Source), OSC UNIT:dBm to set the OSC level unit to dBm.
6. Set the controls as follows:

Control Settings	Key Strokes
Frequency: 1 MHz	(Sweep Setup), CLEAR LIST, YES, ADD, FREQ, (1), (M/μ), SEGMENT DONE, LIST DONE
OSC Level: −19 dBm	(Source), OSC LEVEL, (−), (1), (9), (x1)

7. Subtract −19 dBm (HP 4286A setting) from the power meter reading, and record the result on the performance test record.
8. Change the HP 4286A OSC level using (Source), OSC LEVEL and numeric keys, and change the HP 4286A frequency setting using (Sweep Setup), EDIT, FREQ and numeric keys to test the HP 4286A at the following test points:

Table 2-1. OSC Level Accuracy Test Setting for 1 m Test Head

OSC Level	Center Frequency
−19 dBm	1 MHz
−13 dBm	10 MHz
−7 dBm	100 MHz
7 dBm	500 MHz
1 dBm	1 GHz
7 dBm	1 GHz

Table 2-2. OSC Level Accuracy Test Setting for 3 m Test Head

OSC Level	Center Frequency
−19 dBm	1 MHz
−13 dBm	10 MHz
−7 dBm	100 MHz
7 dBm	500 MHz

MEASUREMENT ACCURACY TEST

Description

In this test, calibrated standards (from the HP 16190A Performance Test Kit) are measured with the HP 4286A. The items tested are 1) Impedance Measurement Accuracy and 2) DC Resistance Measurement Accuracy (for the contact check function). Measurement results of both impedance and DC resistance are displayed simultaneously with one trigger.

Test Equipment

Performance Test Kit ..... HP 16190A
3/4 inch Torque Wrench, 136 N-cm ..... PN 8710-1766
APC7 Calibration Kit ..... HP 16195A[1]
APC3.5(m)-APC7 Adapter ..... PN 1250-1746[2]
APC3.5(m)-APC3.5(f) Right Angle Adapter ..... PN 1250-1249[3]
Test Fixture Stand ..... PN 04286-60141[2]

[1]: Required for testing the HP 4286A of option 001 Delete APC7 Calibration Kit.
[2]: HP 4286A furnished accessory
[3]: HP 4286A option 021/022 furnished accessory

Note

- DC resistance measurement accuracy is tested under the following conditions: Standard:SHORT/50 Ω, OSC level:1 V. Under other test conditions, ignore the DC resistance readings.
- If the HP 16190A 50 Ω standard has no DC calibrated value for the DC resistance measurement accuracy test, use its 1 MHz calibrated value instead.

Procedure

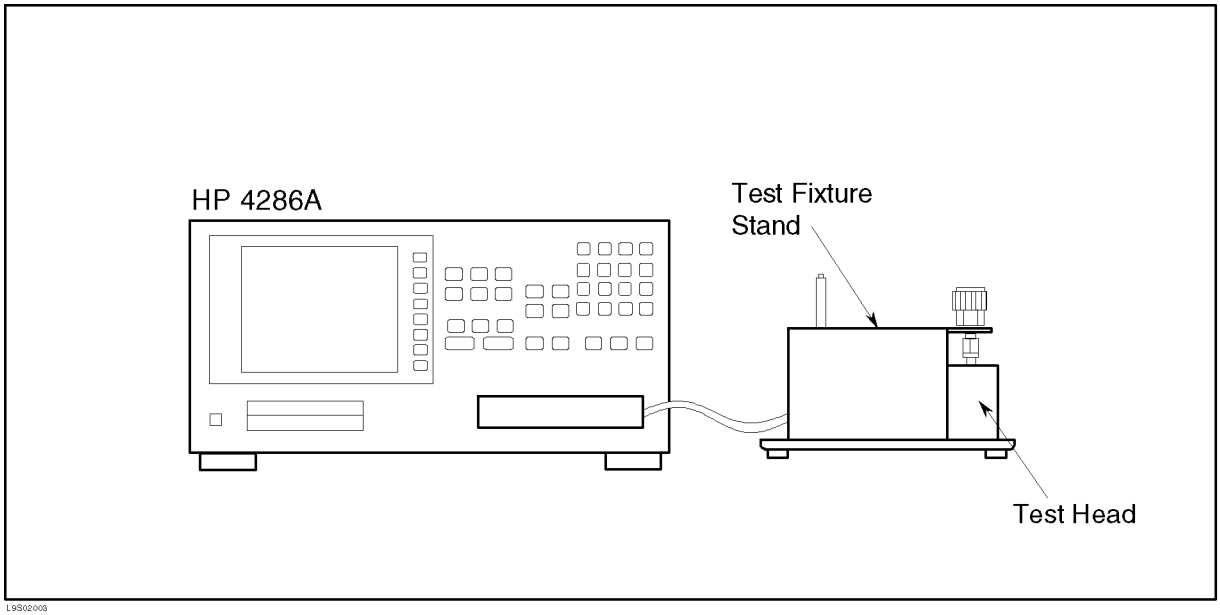


Figure 2-3. Impedance Measurement Accuracy Test Setup

1. Connect the test head to the main frame, and set the test head on the test fixture stand. Then connect the APC3.5(m)-APC7 adapter to the test head. In the case of option 021/022 (Straight Angle Test Head), use the APC3.5(m)-APC3.5(f) right angle adapter to connect the APC3.5(m)-APC7 adapter to the test head. See Figure 2-3.
2. Press (Preset) to initialize the HP 4286A.
3. Create the sweep list shown in Figure 2-4, using the following procedure:

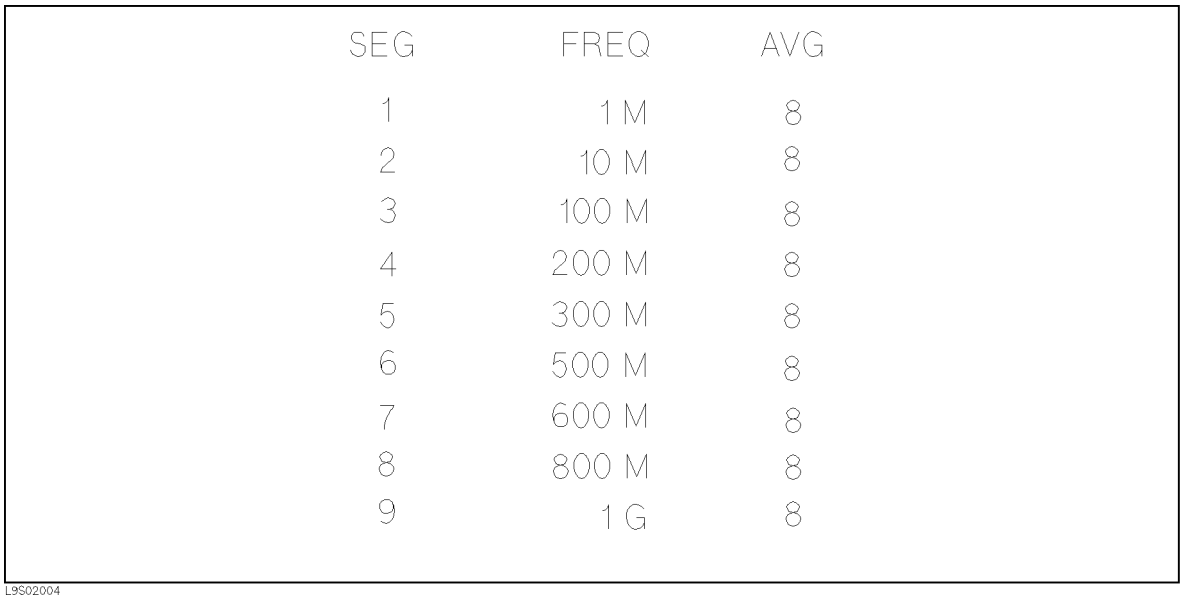


Figure 2-4. Sweep List for Measurement Accuracy Test

a. Press (Sweep Setup), CLEAR LIST, YES.

b. Edit the first segment as follows:

Control Settings	Key Strokes
Frequency: 1 MHz	ADD, FREQ, (1), (M/μ)
Averaging on Point: 8	AVERAGING ON POINT, (8), (x1)

c. Press SEGMENT DONE to store the segment.

d. Press ADD to display the second segment. Then edit the segment in the same manner.

e. Edit all the necessary segments. Then press LIST DONE to complete the sweep list.

Calibrating the HP 4286A

Note

- Calibration must be done using the HP 4286A furnished calibration kit. Or, in the case of the HP 4286A option 001 (Delete APC7 Calibration Kit), calibration must be done using the stand alone HP 16195A APC7 Calibration Kit. Do not use the HP 16190A performance test kit for calibration.
- Calibration must be done when the HP 4286A is turned ON because calibration data is erased when it is turned OFF.
- Do not perform the low-loss capacitor calibration, (the HP 4286A performance is specified without low-loss capacitor calibration).

1. Press (Cal), `CALIBRATE MENU`.
2. Press `CAL POINTS [user]` and verify the softkey label changes to `CAL POINT [fixed]`.
3. Connect the 0 S termination of the APC7 calibration kit to the test head. Then press `OPEN` to do the open calibration.
4. Disconnect the 0 S termination, and connect the 0 Ω termination. Then press `SHORT` to do the short calibration.
5. Disconnect the 0 Ω termination, and connect the 50 Ω termination. Then press `LOAD` to do the load calibration.
6. Press `DONE CAL` to complete the calibration.

Turning on the DC Resistance Measurement Function

7. Press (Contact Check), `RDC MEAS on OFF` and verify the softkey label changes to `RDC MEAS ON off`. The DC resistance measurement value is displayed.

Open Measurement Test

8. Record the open termination calibration values on the performance test record.
9. Connect the open termination to the test head, and torque the connection to 136 N-cm.
10. Press (meas), `|Y|-θrad` to set the measurement parameter to |Y|-θrad.
11. Press `OSC LEVEL`, (1), (x1) to set the OSC level to 1 V.
12. Press (Trigger Mode), `TRIGGER[]`, `MANUAL`, `RETURN` to set the HP 4286A to manual trigger mode.
13. Press (Trigger) to measure.
14. Subtract the open calibrated values from the HP 4286A "|Y|" display values. Then record the test results on the performance test record.
15. Press (Source), `OSC LEVEL`, (.), (2) to set the OSC level to 200 mV.
16. Press (Trigger) to measure.
17. Subtract the open calibrated values from the HP 4286A "|Y|" display values. Then record the test results on the performance test record.

Short Measurement Test

18. Record the short termination calibration values on the performance test record.
19. Connect the short termination to the test head, and torque the connection to 136 N-cm.
20. Press (Meas), |Z|-θrad to set the measurement parameter to |Z|-θrad.
21. Press (Source), OSC LEVEL, (1), (x1) to set the OSC level to 1 V.
22. Press (Trigger), SINGLE to measure.
23. Subtract the short calibrated values from the HP 4286A "|Z|" display values, and record the test results on the performance test record.
24. Record the HP 4286A DC resistance display value on the performance test record.
25. Press (Source), OSC LEVEL, (.), (2), (x1) to set the OSC level to 200 mV.
26. Press (Trigger) to measure.
27. Subtract the short calibrated values from the HP 4286A "|Z|" display values, and record the test results on the performance test record.

50 Ω Measurement Test

28. Record the 50 Ω termination calibration values on the performance test record.
29. Connect the 50 Ω termination to the test head, and torque the connection to 136 N-cm.
30. Press (Source), OSC LEVEL, (1), (x1) to set the OSC level to 1 V.
31. Press (Trigger) to measure.
32. Subtract the 50 Ω "|Z|, θrad" calibrated values from the HP 4286A "|Z|, θrad" display values, and record the test results on the performance test record.
33. Subtract the 50 Ω DC calibrated values from the HP 4286A DC resistance display value, and record the test result on the performance test record.
34. Press (Source), OSC LEVEL, (.), (2), (x1) to set the OSC level to 200 mV.
35. Press (Trigger) to measure.
36. Subtract the 50 Ω calibrated values from the HP 4286A "|Z|, θrad" display values, and record the test results on the performance test record.

10 cm Airline with Open Test

37. Record the 10 cm airline with open termination calibration values on the performance test record.
38. Connect the 10 cm airline and open termination to the test head, using the following procedures (see Figure 2-5).
    a. Fully retract the threads on the test head APC7 connector. Then insert the marked side tip of the airline center conductor into the connector center conductor.
    b. Gently cover the airline center conductor with the airline outer conductor (with the HP logo side down). (To prevent damage, do not let the center conductor scrape the edge of the outer conductor.) Mate the outer conductors. Then torque the connection to 136 N-cm. (A 1/2 inch open end wrench may be necessary to hold the airline stationary.)

c. Gently inserts the airline center conductor into the open termination center conductor. Mate the outer conductors. Then torque the connection to 136 N-cm.

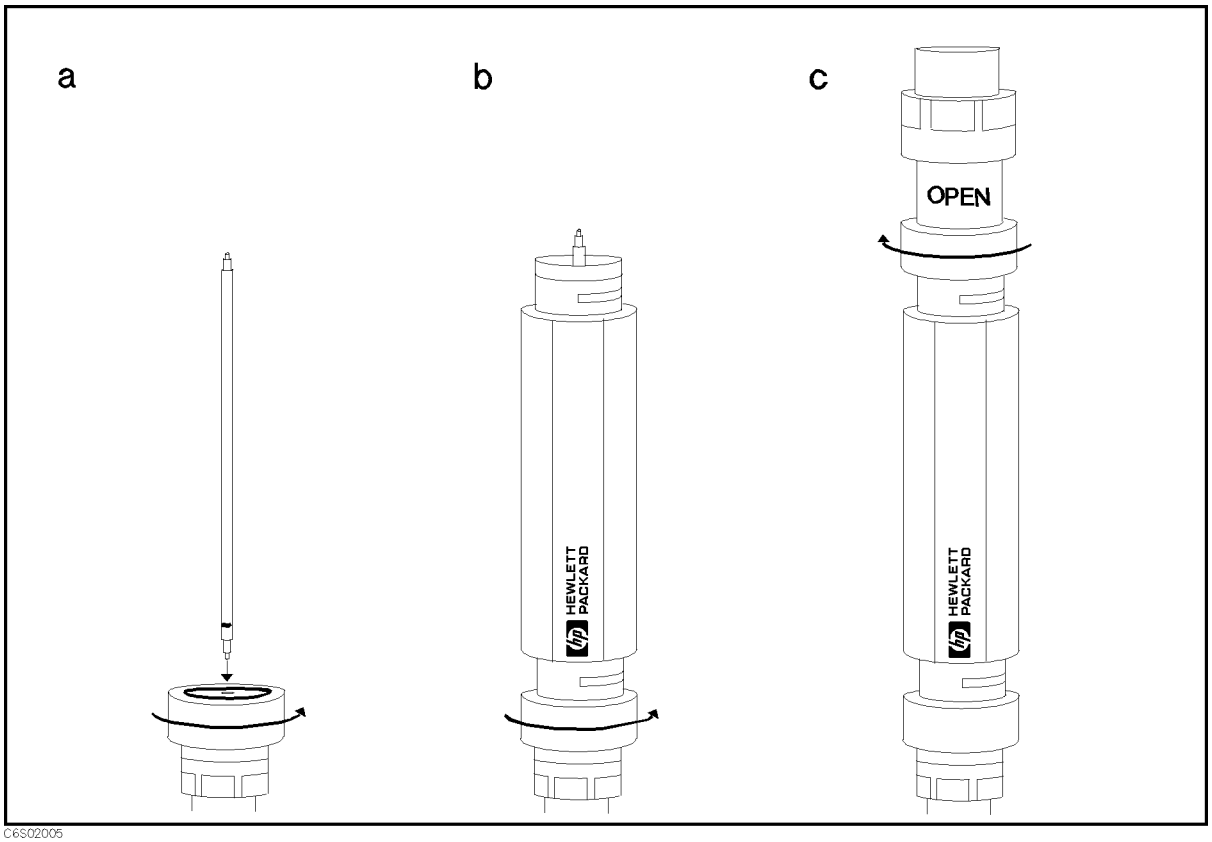


Figure 2-5. 10 cm Airline with Open Measurement Test Setup

39. Press (Source), OSC LEVEL, (1), (x1) to set the OSC level to 1 V.
40. Press (Trigger) to measure.
41. Subtract the 10 cm airline with open calibrated values from the HP 4286A "|Z|, θrad" display values, and record the test results on the performance test record.
42. Press (Source), OSC LEVEL, (.), (2), (x1) to set the OSC level to 200 mV.
43. Press (Trigger) to measure.
44. Subtract the 10 cm airline with open calibrated values from the HP 4286A "|Z|, θrad" display values, and record the test results on the performance test record.

10 cm Airline with Short Test

45. Record the 10 cm airline with short termination calibration values on the performance test record.

46. Connect the 10 cm airline and short termination to the test head APC-7 connector, using the following procedures (see Figure 2-6).

    a. Remove the open termination from the airline.

    b. Gently inserts the airline center conductor into the short termination center conductor. Mate the outer conductors. Then torque the connection to 136 N-cm. (A 1/2 inch open end wrench may be necessary to hold the airline stationary.)

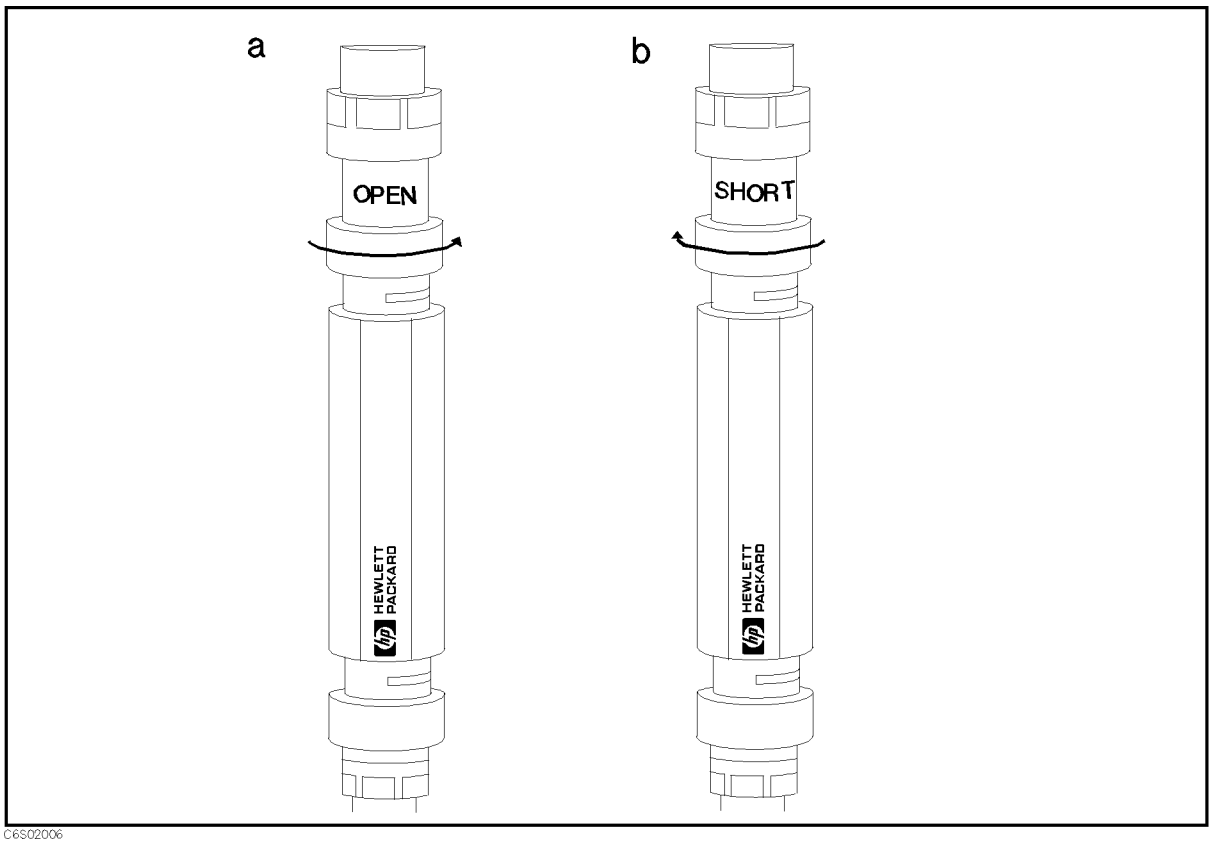


Figure 2-6. 10 cm Airline with Short Measurement Test Setup

47. Press (Source), OSC LEVEL, (1), (x1) to set the OSC level to 1 V.

48. Press (Trigger) to measure.

49. Subtract the 10 cm airline with short calibrated values from the HP 4286A "|Z|, θrad" display values. Then record the test results on the performance test record. (Ignore the HP 4286A display values at 800 MHz.)

50. Press (Source), OSC LEVEL, (.), (2), (x1) to set the OSC level to 200 mV.

51. Press (Trigger) to measure.

52. Subtract the 10 cm airline with short calibrated values from the HP 4286A "|Z|, θrad" display values. Then record the test results on the performance test record. (Ignore the HP 4286A display values at 800 MHz.)

PERFORMANCE TEST RECORD

Hewlett-Packard 4286A RF LCR Meter

Serial No.	Mainframe	_____	Test Date	_____
	Test Head	_____	Temperature	_____
	APC7 Calibration Kit	_____	Humidity	_____
	Tested by:	_____		

Frequency Accuracy Test

Frequency	Test Limit	Test Result	Measurement Uncertainty
1 GHz	± 10.0 kHz	_____ kHz	±2.3 kHz

Osc Level Accuracy Test

1 m Test Head (Standard / Option 031)

Osc Level	Frequency	Test Limit	Test Result	Measurement Uncertainty
−19 dBm	1 MHz	±3.00 dB	_____ dB	±0.18 dB
−13 dBm	10 MHz	±3.00 dB	_____ dB	±0.19 dB
−7 dBm	100 MHz	±3.00 dB	_____ dB	±0.20 dB
7 dBm	500 MHz	±2.00 dB	_____ dB	±0.21 dB
1 dBm	1 GHz	±2.00 dB	_____ dB	±0.20 dB
7 dBm	1 GHz	±2.00 dB	_____ dB	±0.20 dB

3 m Test Head (Option 022/032)

Osc Level	Frequency	Test Limit	Test Result	Measurement Uncertainty
−19 dBm	1 MHz	±3.00 dB	_____ dB	±0.18 dB
−13 dBm	10 MHz	±3.00 dB	_____ dB	±0.19 dB
−7 dBm	100 MHz	±3.00 dB	_____ dB	±0.20 dB
7 dBm	500 MHz	±2.00 dB	_____ dB	±0.21 dB

Measurement Accuracy Test

(1) Impedance Measurement Accuracy Test

Standard: Open
Osc Level: 1 V

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Y|	_____ μS	±30.2 μS	_____ μS	±34 nS
10 MHz	|Y|	_____ μS	±32.3 μS	_____ μS	±0.34 μS
100 MHz	|Y|	_____ μS	±52.7 μS	_____ μS	±3.4 μS
200 MHz	|Y|	_____ μS	±76.6 μS	_____ μS	±6.7 μS
300 MHz	|Y|	_____ mS	±100 μS	_____ μS	±10.0 μS
500 MHz	|Y|	_____ mS	±147 μS	_____ μS	±16.7 μS
600 MHz	|Y|	_____ mS	±181 μS	_____ μS	±21 μS
800 MHz	|Y|	_____ mS	±233 μS	_____ μS	±28 μS
1 GHz	|Y|	_____ mS	±286 μS	_____ μS	±35 μS

Standard: Open
Osc Level: 200 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Y|	_____ μS	±30.2 μS	_____ μS	±34 nS
10 MHz	|Y|	_____ μS	±32.3 μS	_____ μS	±0.34 μS
100 MHz	|Y|	_____ μS	±53.2 μS	_____ μS	±3.4 μS
200 MHz	|Y|	_____ μS	±77.6 μS	_____ μS	±6.7 μS
300 MHz	|Y|	_____ mS	±101 μS	_____ μS	±10.0 μS
500 MHz	|Y|	_____ mS	±150 μS	_____ μS	±16.7 μS
600 MHz	|Y|	_____ mS	±184 μS	_____ μS	±21 μS
800 MHz	|Y|	_____ mS	±237 μS	_____ μS	±28 μS
1 GHz	|Y|	_____ mS	±291 μS	_____ μS	±35 μS

Standard: Short
Osc Level: 1 V

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	0.00 mΩ	±20.5 mΩ	_____ mΩ	±1.8 mΩ
10 MHz	|Z|	0.00 mΩ	±25.0 mΩ	_____ mΩ	±2.0 mΩ
100 MHz	|Z|	0.00 mΩ	±70.0 mΩ	_____ mΩ	±10 mΩ
200 MHz	|Z|	0.00 mΩ	±120 mΩ	_____ mΩ	±20 mΩ
300 MHz	|Z|	0.00 mΩ	±170 mΩ	_____ mΩ	±30 mΩ
500 MHz	|Z|	0.00 mΩ	±270 mΩ	_____ mΩ	±40 mΩ
600 MHz	|Z|	0.00 mΩ	±320 mΩ	_____ mΩ	±50 mΩ
800 MHz	|Z|	0.00 mΩ	±420 mΩ	_____ mΩ	±70 mΩ
1 GHz	|Z|	0.00 mΩ	±520 mΩ	_____ mΩ	±80 mΩ

Standard: Short
Osc Level: 200 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	0.00 mΩ	±20.5 mΩ	_____ mΩ	±1.8 mΩ
10 MHz	|Z|	0.00 mΩ	±25.0 mΩ	_____ mΩ	±2.0 mΩ
100 MHz	|Z|	0.00 mΩ	±70.0 mΩ	_____ mΩ	±10.0 mΩ
200 MHz	|Z|	0.00 mΩ	±120 mΩ	_____ mΩ	±20 mΩ
300 MHz	|Z|	0.00 mΩ	±170 mΩ	_____ mΩ	±30 mΩ
500 MHz	|Z|	0.00 mΩ	±270 mΩ	_____ mΩ	±40 mΩ
600 MHz	|Z|	0.00 mΩ	±320 mΩ	_____ mΩ	±50 mΩ
800 MHz	|Z|	0.00 mΩ	±420 mΩ	_____ mΩ	±70 mΩ
1 GHz	|Z|	0.00 mΩ	±520 mΩ	_____ mΩ	±80 mΩ

Standard: 50 Ω
Osc Level: 1 V

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ Ω	±436 mΩ	_____ mΩ	±90 mΩ
1 MHz	θ	_____ mrad	±8.72 mrad	_____ mrad	±1.80 mrad
10 MHz	|Z|	_____ Ω	±445 mΩ	_____ mΩ	±90 mΩ
10 MHz	θ	_____ mrad	±8.90 mrad	_____ mrad	±1.80 mrad
100 MHz	|Z|	_____ Ω	±535 mΩ	_____ mΩ	±100 mΩ
100 MHz	θ	_____ mrad	±10.7 mrad	_____ mrad	±2.0 mrad
200 MHz	|Z|	_____ Ω	±710 mΩ	_____ mΩ	±125 mΩ
200 MHz	θ	_____ mrad	±14.2 mrad	_____ mrad	±2.5 mrad
300 MHz	|Z|	_____ Ω	±810 mΩ	_____ mΩ	±150 mΩ
300 MHz	θ	_____ mrad	±16.2 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±1.01 Ω	_____ mΩ	±200 mΩ
500 MHz	θ	_____ mrad	±20.2 mrad	_____ mrad	±4.0 mrad
600 MHz	|Z|	_____ Ω	±1.31 Ω	_____ Ω	±0.25 Ω
600 MHz	θ	_____ mrad	±26.2 mrad	_____ mrad	±5.0 mrad
800 MHz	|Z|	_____ Ω	±1.51 Ω	_____ Ω	±0.25 Ω
800 MHz	θ	_____ mrad	±30.2 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±1.71 Ω	_____ Ω	±0.25 Ω
1 GHz	θ	_____ mrad	±34.2 mrad	_____ mrad	±5.0 mrad

Standard: 50 Ω
Osc Level: 200 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ Ω	±496 mΩ	_____ mΩ	±90 mΩ
1 MHz	θ	_____ mrad	±9.92 mrad	_____ mrad	±1.80 mrad
10 MHz	|Z|	_____ Ω	±505 mΩ	_____ mΩ	±90 mΩ
10 MHz	θ	_____ mrad	±10.1 mrad	_____ mrad	±1.80 mrad
100 MHz	|Z|	_____ Ω	±595 mΩ	_____ mΩ	±100 mΩ
100 MHz	θ	_____ mrad	±11.9 mrad	_____ mrad	±2.00 mrad
200 MHz	|Z|	_____ Ω	±770 mΩ	_____ mΩ	±125 mΩ
200 MHz	θ	_____ mrad	±15.4 mrad	_____ mrad	±2.5 mrad
300 MHz	|Z|	_____ Ω	±870 mΩ	_____ mΩ	±150 mΩ
300 MHz	θ	_____ mrad	±17.4 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±1.07 Ω	_____ mΩ	±200 mΩ
500 MHz	θ	_____ mrad	±21.4 mrad	_____ mrad	±4.0 mrad
600 MHz	|Z|	_____ Ω	±1.37 Ω	_____ Ω	±0.25 Ω
600 MHz	θ	_____ mrad	±27.4 mrad	_____ mrad	±5.0 mrad
800 MHz	|Z|	_____ Ω	±1.57 Ω	_____ Ω	±0.25 Ω
800 MHz	θ	_____ mrad	±31.4 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±1.77 Ω	_____ Ω	±0.25 Ω
1 GHz	θ	_____ mrad	±35.4 mrad	_____ mrad	±5.0 mrad

Standard: 10 cm Airline with Open
Osc Level: 1 V

Frequency	Measurement Parameter	Calibration Value		Test Limit	Test Result		Measurement Uncertainty
1 MHz	|Z|	_____	kΩ	±14.5 kΩ	_____	kΩ	±43 Ω
1 MHz	θ	_____	rad	±665 mrad	_____	mrad	±2.0 mrad
10 MHz	|Z|	_____	kΩ	±167 Ω	_____	Ω	±4.3 Ω
10 MHz	θ	_____	rad	±76.6 mrad	_____	mrad	±2.0 mrad
100 MHz	|Z|	_____	Ω	±3.82 Ω	_____	Ω	±0.43 Ω
100 MHz	θ	_____	rad	±17.8 mrad	_____	mrad	±2.0 mrad
200 MHz	|Z|	_____	Ω	±1.68 Ω	_____	Ω	±0.25 Ω
200 MHz	θ	_____	rad	±16.6 mrad	_____	mrad	±2.5 mrad
300 MHz	|Z|	_____	Ω	±1.01 Ω	_____	mΩ	±182 mΩ
300 MHz	θ	_____	rad	±16.6 mrad	_____	mrad	±3.0 mrad
500 MHz	|Z|	_____	Ω	±523 mΩ	_____	mΩ	±90 mΩ
500 MHz	θ	_____	rad	±23.2 mrad	_____	mrad	±4.0 mrad
600 MHz	|Z|	_____	Ω	±455 mΩ	_____	mΩ	±88 mΩ
600 MHz	θ	_____	rad	±46.4 mrad	_____	mrad	±9.0 mrad
800 MHz	|Z|	_____	Ω	±622 mΩ	_____	mΩ	±122 mΩ
800 MHz	θ	_____	rad	±45.8 mrad	_____	mrad	±9.0 mrad
1 GHz	|Z|	_____	Ω	±1.51 Ω	_____	Ω	±0.27 Ω
1 GHz	θ	_____	rad	±34.2 mrad	_____	mrad	±6.0 mrad

Standard: 10 cm Airline with Open
Osc Level: 200 mV

Frequency	Measurement Parameter	Calibration Value		Test Limit	Test Result		Measurement Uncertainty
1 MHz	|Z|	_____	kΩ	±14.5 kΩ	_____	kΩ	±43 Ω
1 MHz	θ	_____	rad	±667 mrad	_____	mrad	±2.0 mrad
10 MHz	|Z|	_____	kΩ	±170 Ω	_____	Ω	±4.3 Ω
10 MHz	θ	_____	rad	±77.8 mrad	_____	mrad	±2.0 mrad
100 MHz	|Z|	_____	Ω	±4.08 Ω	_____	Ω	±0.43 Ω
100 MHz	θ	_____	rad	±19.0 mrad	_____	mrad	±2.0 mrad
200 MHz	|Z|	_____	Ω	±1.80 Ω	_____	Ω	±0.25 Ω
200 MHz	θ	_____	rad	±17.8 mrad	_____	mrad	±2.5 mrad
300 MHz	|Z|	_____	Ω	±1.08 Ω	_____	mΩ	±182 mΩ
300 MHz	θ	_____	rad	±17.8 mrad	_____	mrad	±3.0 mrad
500 MHz	|Z|	_____	Ω	±550 mΩ	_____	mΩ	±90 mΩ
500 MHz	θ	_____	rad	±24.4 mrad	_____	mrad	±4.0 mrad
600 MHz	|Z|	_____	Ω	±467 mΩ	_____	mΩ	±88 mΩ
600 MHz	θ	_____	rad	±47.6 mrad	_____	mrad	±9.0 mrad
800 MHz	|Z|	_____	Ω	±639 mΩ	_____	mΩ	±122 mΩ
800 MHz	θ	_____	rad	±47.0 mrad	_____	mrad	±9.0 mrad
1 GHz	|Z|	_____	Ω	±1.57 Ω	_____	Ω	±0.27 Ω
1 GHz	θ	_____	rad	±35.4 mrad	_____	mrad	±6.0 mrad

Standard: 10 cm Airline with Short
Osc Level: 1 V

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ mΩ	±21.3 mΩ	_____ mΩ	±1.7 mΩ
1 MHz	θ	_____ rad	±188 mrad	_____ mrad	±15 mrad
10 MHz	|Z|	_____ Ω	±32.3 mΩ	_____ mΩ	±4.3 mΩ
10 MHz	θ	_____ rad	±30.1 mrad	_____ mrad	±4.0 mrad
100 MHz	|Z|	_____ Ω	±149 mΩ	_____ mΩ	±27 mΩ
100 MHz	θ	_____ rad	±13.9 mrad	_____ mrad	±2.5 mrad
200 MHz	|Z|	_____ Ω	±341 mΩ	_____ mΩ	±67 mΩ
200 MHz	θ	_____ rad	±15.2 mrad	_____ mrad	±3.0 mrad
300 MHz	|Z|	_____ Ω	±593 mΩ	_____ mΩ	±110 mΩ
300 MHz	θ	_____ rad	±16.2 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±1.98 Ω	_____ Ω	±0.31 Ω
500 MHz	θ	_____ rad	±22.7 mrad	_____ mrad	±3.5 mrad
600 MHz	|Z|	_____ Ω	±5.85 Ω	_____ Ω	±0.78 Ω
600 MHz	θ	_____ rad	±37.7 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±3.29 Ω	_____ Ω	±0.52 Ω
1 GHz	θ	_____ rad	±38.1 mrad	_____ mrad	±6.0 mrad

Standard: 10 cm Airline with Short
Osc Level: 200 mV

Frequency	Measurement Parameter	Calibration Value	Test Limit	Test Result	Measurement Uncertainty
1 MHz	|Z|	_____ mΩ	±21.4 mΩ	_____ mΩ	±1.7 mΩ
1 MHz	θ	_____ rad	±189 mrad	_____ mrad	±15 mrad
10 MHz	|Z|	_____ Ω	±33.6 mΩ	_____ mΩ	±4.3 mΩ
10 MHz	θ	_____ rad	±31.3 mrad	_____ mrad	±4.0 mrad
100 MHz	|Z|	_____ Ω	±161 mΩ	_____ mΩ	±27 mΩ
100 MHz	θ	_____ rad	±15.1 mrad	_____ mrad	±2.5 mrad
200 MHz	|Z|	_____ Ω	±368 mΩ	_____ mΩ	±67 mΩ
200 MHz	θ	_____ rad	±16.4 mrad	_____ mrad	±3.0 mrad
300 MHz	|Z|	_____ Ω	±637 mΩ	_____ mΩ	±110 mΩ
300 MHz	θ	_____ rad	±17.4 mrad	_____ mrad	±3.0 mrad
500 MHz	|Z|	_____ Ω	±2.09 Ω	_____ Ω	±0.31 Ω
500 MHz	θ	_____ rad	±23.9 mrad	_____ mrad	±3.5 mrad
600 MHz	|Z|	_____ Ω	±6.03 Ω	_____ Ω	±0.78 Ω
600 MHz	θ	_____ rad	±38.9 mrad	_____ mrad	±5.0 mrad
1 GHz	|Z|	_____ Ω	±3.39 Ω	_____ Ω	±0.52 Ω
1 GHz	θ	_____ rad	±39.3 mrad	_____ mrad	±6.0 mrad

(2) DC Resistance Measurement Accuracy Test

Standard: Short
Osc Level: 1 V

Test Limit	Test Result
±25.0 mΩ	Pass [ ] Fail[ ]

Standard: 50 Ω
Osc Level: 1 V

Calibration Value	Test Limit	Test Result	Measurement Uncertainty
_____ Ω	±1.80 Ω	_____ Ω	±50 mΩ

3

Adjustments and Correction Constants

INTRODUCTION

This chapter describes the Adjustments and Correction Constants procedures required to ensure that the HP 4286A RF LCR Meter is within its specifications. These adjustments should be performed along with periodic maintenance to keep the HP 4286A in optimum operating condition. The recommended calibration period is 12 months. If proper performance cannot be achieved after the Adjustments and Correction Constants procedures are performed, see Chapter 4.

Note 

The correction constants are empirically derived data that is stored in memory and then recalled to refine the HP 4286A's measurement and to define its operation.

SAFETY CONSIDERATIONS

This manual contains NOTEs, CAUTIONs, and WARNINGs that must be followed to ensure the safety of the operator and to keep the instrument in a safe and serviceable condition. The adjustments must be performed by qualified service personnel.

Warning 

Any interruption of the protective ground conductor (inside or outside the HP 4286A) or disconnection of the protective ground terminal can make the instrument dangerous. Intentional interruption of the protective ground system for any reason is prohibited.

The removal or opening of covers for adjustment, or removal of parts other than those that are accessible by hand will expose circuits containing dangerous voltage levels.

Remember that the capacitors in the HP 4286A can remain charged for several minutes, even through you have turned the HP 4286A OFF and unplugged it.

Warning 

The adjustments described in this chapter are performed with power applied and the protective covers removed. Dangerous voltage levels exist at many points and can result in serious personal injury or death if you come into contact with them.

REQUIRED EQUIPMENT

Table 1-1 lists the equipment required to perform the Adjustments and the Correction Constants procedures described in this chapter. Use only calibrated test equipment when adjusting the HP 4286A. If the recommended test equipment is not available, equipment whose specifications are equal to, or surpasses those of the recommended test equipment may be used.

WARM-UP FOR ADJUSTMENTS AND CORRECTION CONSTANTS

Warm-up the HP 4286A for at least 30 minute before performing any of the following Adjustments and Correction Constants procedures to ensure proper results and correct instrument operation.

INSTRUMENT COVER REMOVAL

To gain access to the adjustment components, you need to remove the top cover and the side covers. If additional information is required when removing these covers, see Chapter 13.

ORDER OF ADJUSTMENTS

When performing more than one Adjustments or Correction Constants procedure, perform them in the order they appear in this chapter. The procedures are presented in the following order:

- 40 MHz Reference Oscillator Frequency Adjustment
- 520 MHz Level Adjustment
- Comb Generator Adjustment
- Second Local PLL Lock Adjustment
- Source VCXO Adjustment
- Third Local VCXO Adjustment
- Source Mixer Local Leakage Adjustment
- OSC Level Correction Constants
- Hold Step Adjustment
- Band Pass Filter Adjustment

ADJUSTMENT PROGRAM

This section provides general information about the HP 4286A adjustment program that is used for updating the OSC Level Correction Constants.
The adjustment program is provided on one double-sided diskette. The diskette's HP part number is 04286-65002 . The files contained on the diskette are as follows:

ADJ4286A	Adjustments Program
TE_A4286A	Equipment Configuration Program

Note

To prevent accidental deletion or destruction of the program, make working copies of the furnished master diskette (HFS or SRM system). Use the working copies for daily use. Keep the master diskettes in a safe place and use them only for making working copies.

Keyboard and Mouse Operation

The menus in "ADJ4286A" use a window format. The window format menu supports keyboard and mouse operations as follows:

- Keyboard Operation
  1. Press (▲), (▼) keys until your preference is highlighted.
  2. Choose the highlighted item by pressing (RETURN) or (SELECT) ((ENTER) or (EXECUTE), on a Nimitz Keyboard).
  3. If `QUIT` or `EXIT` is displayed in a menu, select one of these to exit the menu. Otherwise, press (▶) ((CONTINUE), on a Nimitz Keyboard) to exit. When you exit a menu, the program displays another menu.

Note

Press (?) to access on-screen help information for the selection you have highlighted. Help information appears in a display window.

Press (RETURN) or (SELECT) ((ENTER) or (EXECUTE), on a Nimitz Keyboard) to turn off the help screen.

- Mouse Operation
  1. Slide the mouse up or down until your preference is highlighted.
  2. Choose the highlighted item by pressing left-hand button on the mouse, or slide the mouse to the right.
  3. If `QUIT` or `EXIT` is displayed in a menu, select one of these to exit the menu. Otherwise, slide the mouse to the left to exit. When you exit a menu, the program displays another menu.

Note

Press the right-hand mouse button to access on-screen help information for the selection you have highlighted. Help information appears in a display window.

Press the left-hand mouse button to turn off the help screen.

Controller Requirement

The following controller system is required to run the adjustments program.

Controller	HP 9000 Series 200/300 computer.
	Excluding HP 9826A computers.
	Must have inverse video capability.
	At least 4 M bytes of RAM.
Mass Storage	At least one 3.5 inch HP-IB Flexible Disk Drive.
	HFS formatted hard disk system or SRM system are supported.

The controller must be equipped with an HP BASIC version between 5.1 and 5.13, and have the language extension files listed in Table 3-1.

Table 3-1. Required Binaries

Name	Version	Description
GRAPH	5.2	Graphics
GRAPHX	5.2	Graphics Extensions
IO	5.1	I/O
MAT	5.1	Matrix Statements
PDEV	5.0	Program Development
KBD	5.1	Keyboard Extensions
CLOCK	5.0	Clock
MS	5.1	Mass Storage
ERR	5.1	Error Message
DISC	5.0	Small Disc Driver
CS80	5.0	CS80 Disc Driver
HPIB	5.0	HP-IB Interface Driver
FHPIB	5.0	HP-IB Interface Driver
CRTB	5.2	Bit-mapped CRT Driver
CRTA	5.1	Alpha CRT Driver
CRTX	5.1	CRT Extensions
EDIT	5.1	List and Edit
SRM	5.1	Shared Resource Management
DCOMM	5.0	Datacomm Interface Driver
HFS	5.3	Hierarchical File System
COMPLEX	5.1	Complex Arithmetic

Preparation for Using the Adjustment Program

Before using the HP 4286A Adjustment Program, it is necessary to run the program "TE_A4286A" to define the types and HP-IB addresses of the equipment used in the adjustment. Once you set the types and HP-IB addresses of the equipment using the "TE_A4286A", you don't have to perform the "TE_A4286A" for adjustment. The procedure is as follows.

Note

The program "TE_A4286A" must be located at the address of the drive or the directory where the Adjustment Program "ADJ4286A" will be run.

---

1. Turn the computer and bring up the BASIC system.
2. Set the mass storage unit specifier (MSUS) to the address of the drive or the directory where "TE_A4286A" is located.
3. Load and run "TE_A4286A".
4. As the program instruct, select the types of the power meter/power sensor to be used and enter their HP-IB addresses.

If you want to change the types and HP-IB addresses of the equipment, re-perform the "TE_A4286A".

40 MHz REFERENCE OSCILLATOR FREQUENCY ADJUSTMENT

The purpose of this procedure is to adjust the 40 MHz reference oscillator frequency.

Required Equipment

Frequency Counter ..... HP 5343A Option 001
SMB(f)-BNC(f) adapter ..... PN 1250-1236
BNC cable, 61 cm ..... PN 8120-1839

Procedure

1. Connect the equipment as shown in Figure 3-1. The A5 "CAL OUT" connector location is shown in Figure 3-2. Do not connect anything to the rear panel "EXT REF" input connector.

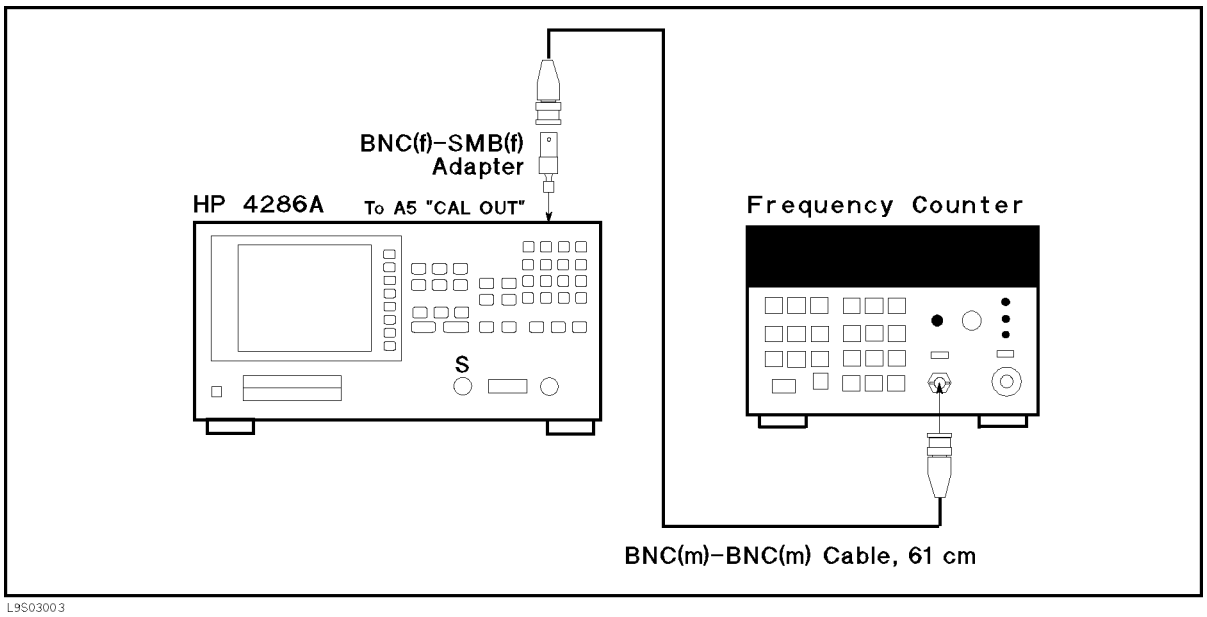


Figure 3-1. 40 MHz Reference Oscillator Frequency Adjustment Setup

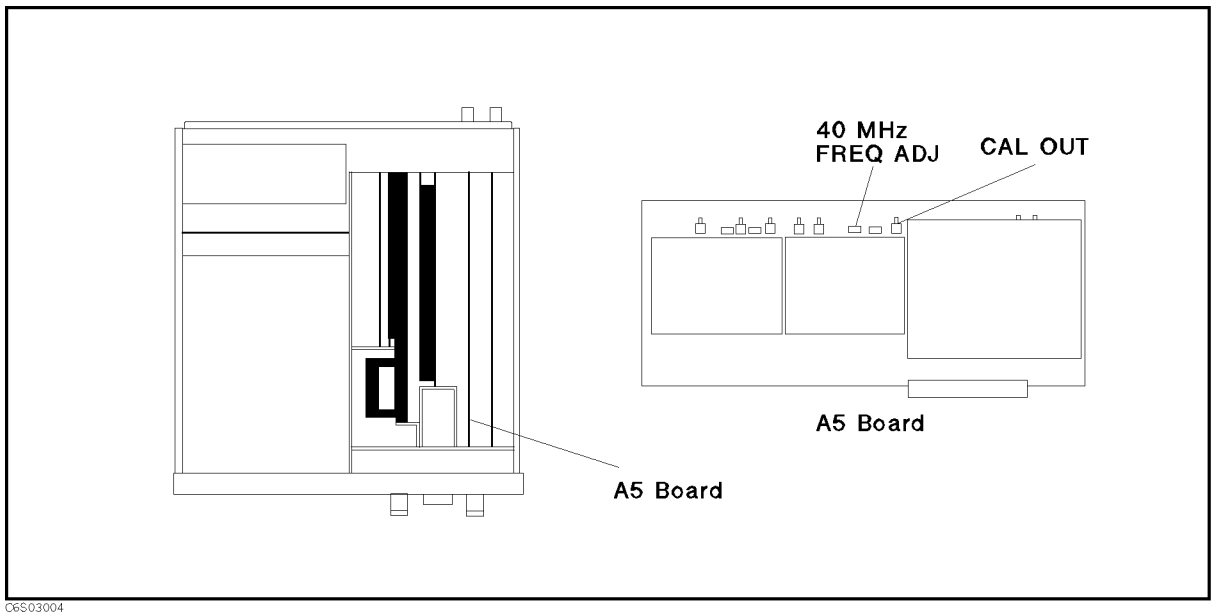


Figure 3-2. 40 MHz Reference Oscillator Frequency Adjustment Location

2. Set the frequency counter as follows:

   Input Impedance 50 Ω
   Frequency Range 10 Hz - 500 MHz

3. Adjust A5 "40 MHz FREQ ADJ" until the frequency counter reading is within 20 MHz ± 20 Hz. The adjustment location is shown in Figure 3-2.

520 MHz LEVEL ADJUSTMENT

The purpose of this procedure is to adjust the 520 MHz output level.

Required Equipment

Spectrum Analyzer ..... HP 8566A/B
SMC(f)-BNC(f) adapter ..... PN 1250-0832
N(m)-BNC(f) adapter ..... PN 1250-1476
BNC cable, 61 cm ..... PN 8120-1839

Procedure

1. Turn the HP 4286A OFF.
2. Remove the "J" cable from the A5 "520 MHz OUT" connector. The connector location is shown in Figure 3-3.

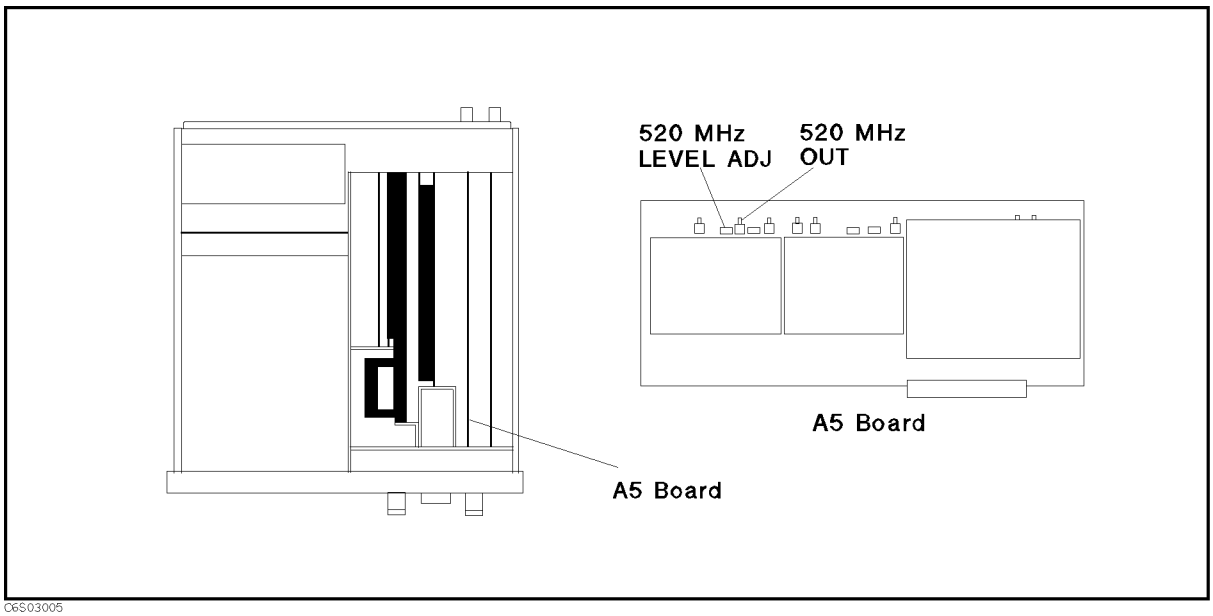


Figure 3-3. 520 MHz Level Adjustment Location

3. Connect the equipment as shown in Figure 3-4.

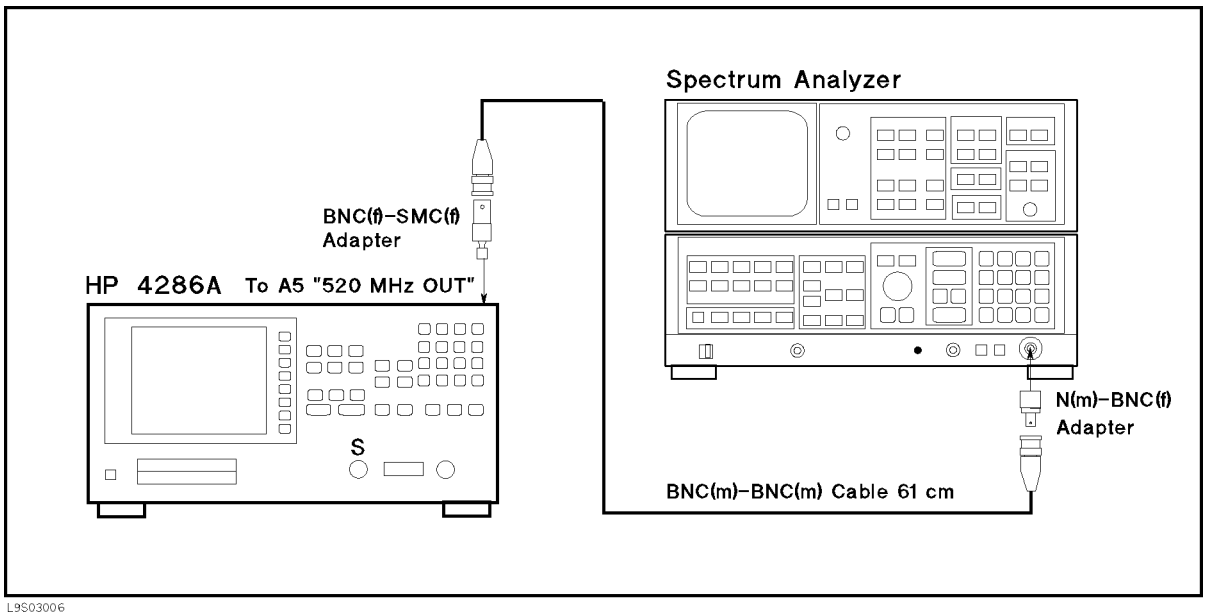


Figure 3-4. 520 MHz Level Adjustment Setup

4. Set the spectrum analyzer as follows:

CENTER Frequency	520 MHz
SPAN	1 MHz
RBW	100 kHz

5. Turn the HP 4286A ON.
6. Adjust A5 “520 MHz LEVEL ADJ” until the spectrum analyzer reading for 520 MHz signal level is within -15 ± 0.2 dBm. The adjustment location is shown in Figure 3-3.
7. Turn the HP 4286A OFF.
8. Reconnect the “J” cable to the A5 “520 MHz OUT” connector.

COMB GENERATOR ADJUSTMENT

The purpose of this procedure is to adjust the comb generator output level.

Required Equipment

Spectrum Analyzer	HP 8566A/B
SMB(f)-BNC(f) adapter	PN 1250-1236
N(m)-BNC(f) adapter	PN 1250-1476
BNC cable, 122 cm	PN 8120-1840

Procedure

1. Turn the HP 4286A OFF.
2. Remove the SMB connector termination from the A5 “COMB OUT” connector, and connect the equipment as shown in Figure 3-5. The A5 “COMB OUT” connector location is shown in Figure 3-6.

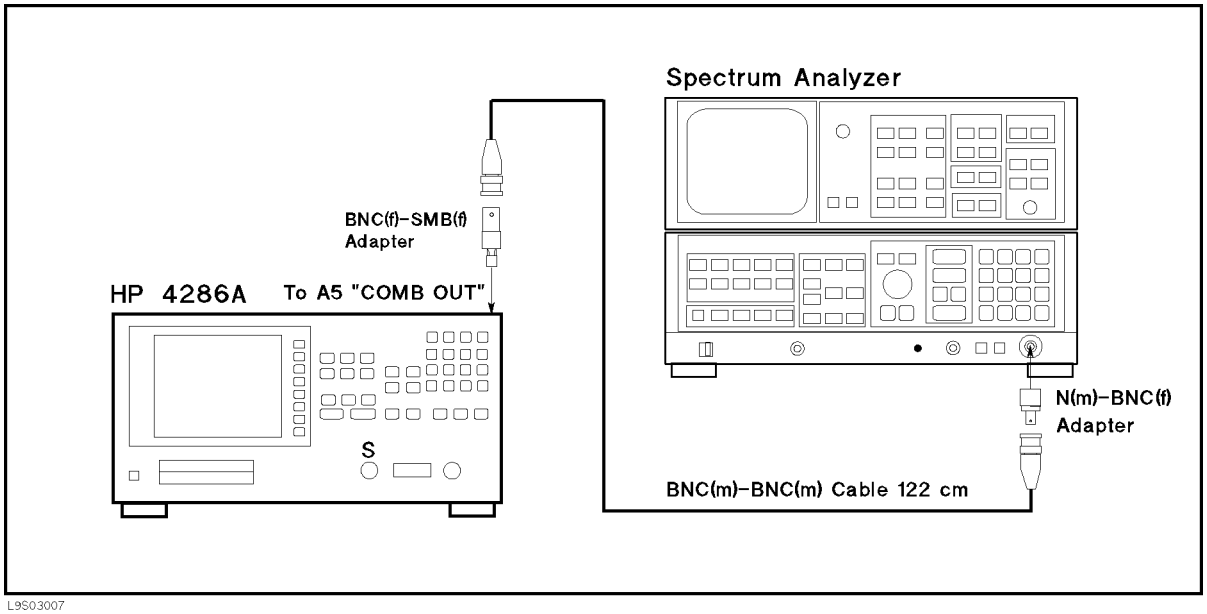


Figure 3-5. Comb Generator Adjustment Setup

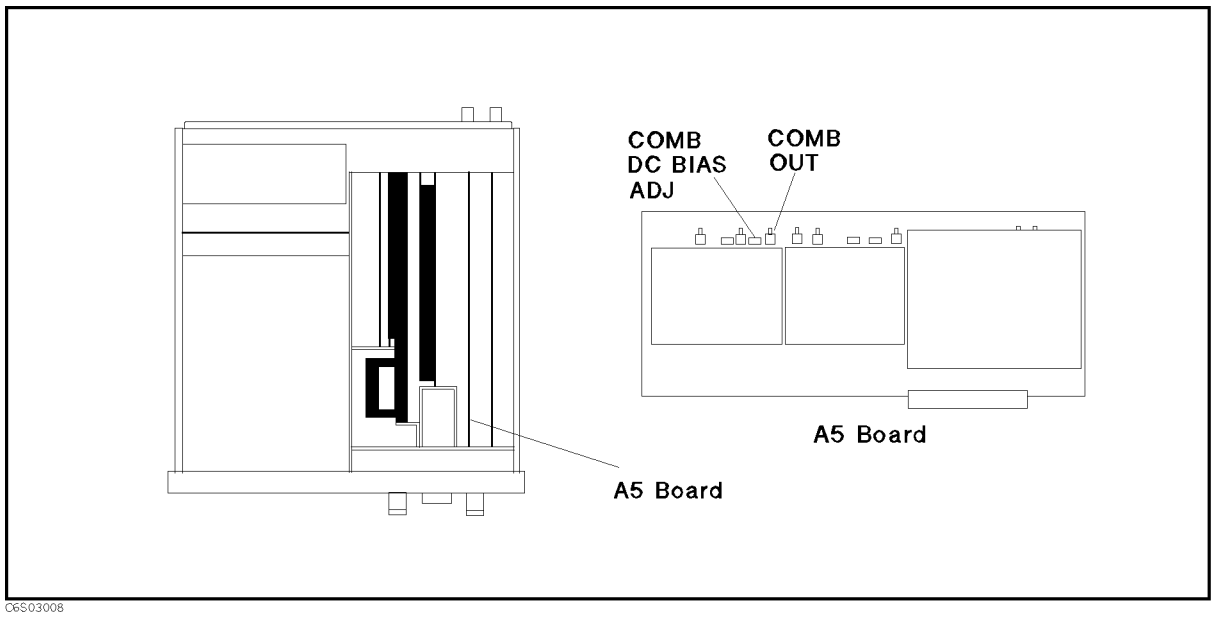


Figure 3-6. Comb Generator Adjustment Location

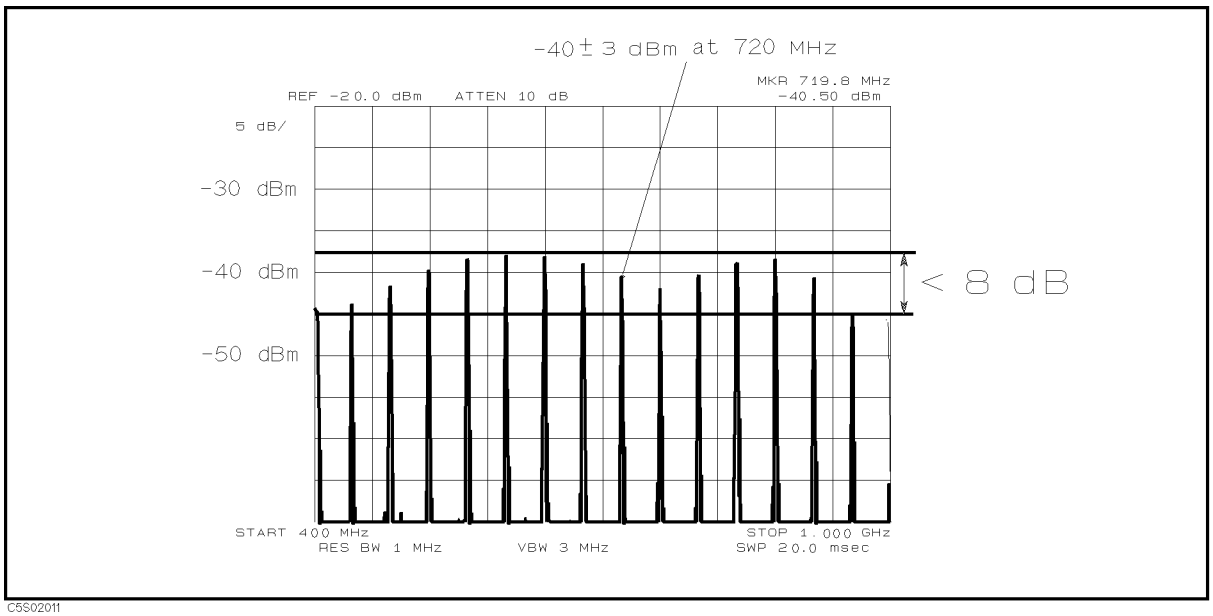
3. Set the spectrum analyzer as follows:

Start Frequency	400 MHz
Stop Frequency	1 GHz
RBW	1 MHz
Reference Level	−20 dBm
Scale	5 dB/div

4. Turn the HP 4286A ON.
5. Adjust A5 “COMB DC BIAS ADJ” until the spectrum analyzer display indicates the following:

720 MHz Signal Level	-40 ± 3 dBm
480 MHz to 920 MHz Flatness	< 8 dB

The adjustment location is shown in Figure 3-6. A typical spectrum analyzer display is shown in Figure 3-7.



C5S02011

Figure 3-7. Comb Generator Output

SECOND LOCAL PLL LOCK ADJUSTMENT

The purpose of this procedure is to lock the second local Phase Lock Loop (PLL).

Required Equipment

Spectrum Analyzer	HP 8566A/B
BNC(f)-SMA(m) adapter	PN 1250-1548
N(m)-BNC(f) adapter	PN 1250-1476
BNC cable, 122 cm	PN 8120-1840

Procedure

1. Turn the HP 4286A OFF.
2. Remove the "D" cable from the A3A1 "ALC Out" connector. Remove the "I" cable from the A3A2 "Second Local Out" connector. The connector locations are shown in Figure 3-8.

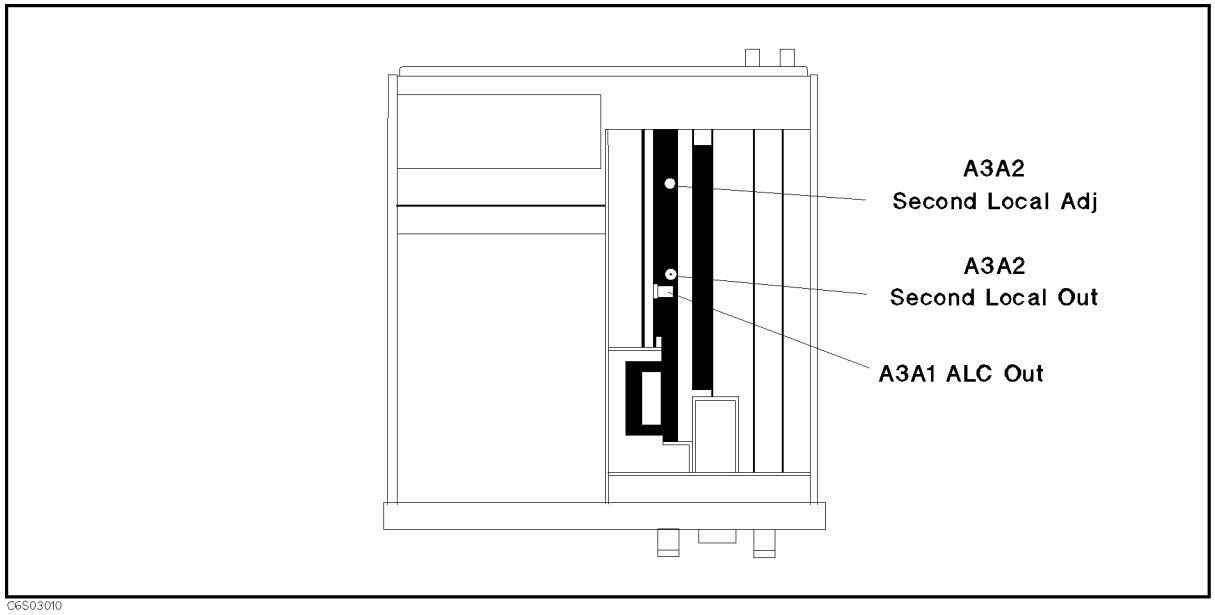


Figure 3-8. Second Local PLL Adjustment Location

3. Connect the equipment as shown in Figure 3-9.

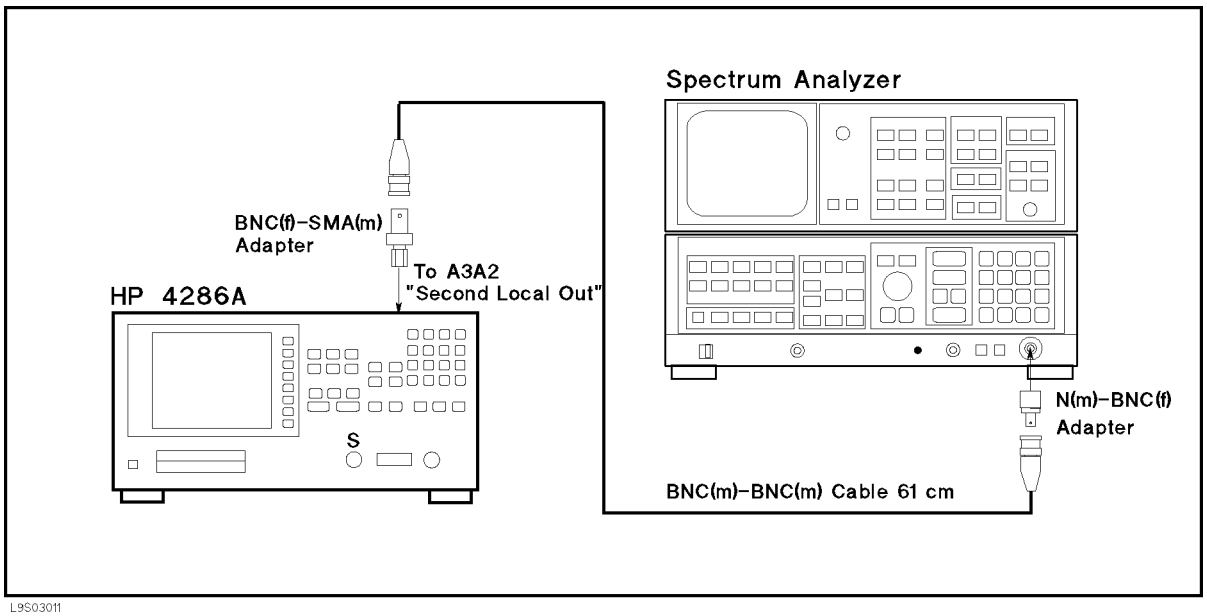


Figure 3-9. Second Local PLL Adjustment Setup

4. Set the spectrum analyzer as follows:

Center Frequency	2.08 GHz
Span	400 MHz
RBW	1 MHz

5. Turn the HP 4286A ON.
6. Press the following keys to execute adjustment test No.29:

   (PRESET), (SYSTEM), SERVICE MENU, TESTS, (2), (9), (x1), EXECUTE TEST
   The tuning voltage of the second local oscillator is displayed in the "R: " field.
7. Adjust A3A2 "Second Local Adj" until 2.08 GHz appears constantly on the spectrum analyzer display and the HP 4286A reading is within 0 ± 8 mU. Then press CONT to complete the adjustment. If 2.24 GHz appears, rotate "Second Local Adj" clockwise. If 1.92 GHz appears, rotate "Second Local Adj" counterclockwise. The adjustment location is shown in Figure 3-8.
8. Turn the HP 4286A OFF.
9. Reconnect the "I" cable to the A3A2 "Second Local Out" connector. Reconnect the "D" cable to the A3A1 "ALC Out" connector.

SOURCE VCXO ADJUSTMENT

The purpose of this procedure is to optimize the source VCXO oscillation.

Required Equipment

None

Procedure

1. Do not connect anything to the HP 4286A mainframe front terminals.
2. Press the following keys to execute adjustment test No.31:
   (PRESET), (SYSTEM), SERVICE MENU , TESTS , (3), (1), (x1), EXECUTE TEST
   The VCXO output level is displayed in the "R :" field
3. Rotate "VCXO LEV" and confirm that a voltage peak appears in a rotation to confirm that the VCXO circuit is correct. Then press CONT .
4. Rotate "VCXO LEV" slowly to enable instrument to memorize the peak voltage. Then press CONT .
5. Adjust "VCXO LEV" until the VCXO level is within the limits and "PASS" is displayed. The limit is the memorized peak voltage +0/-1 %. Then press CONT to complete the adjustment.

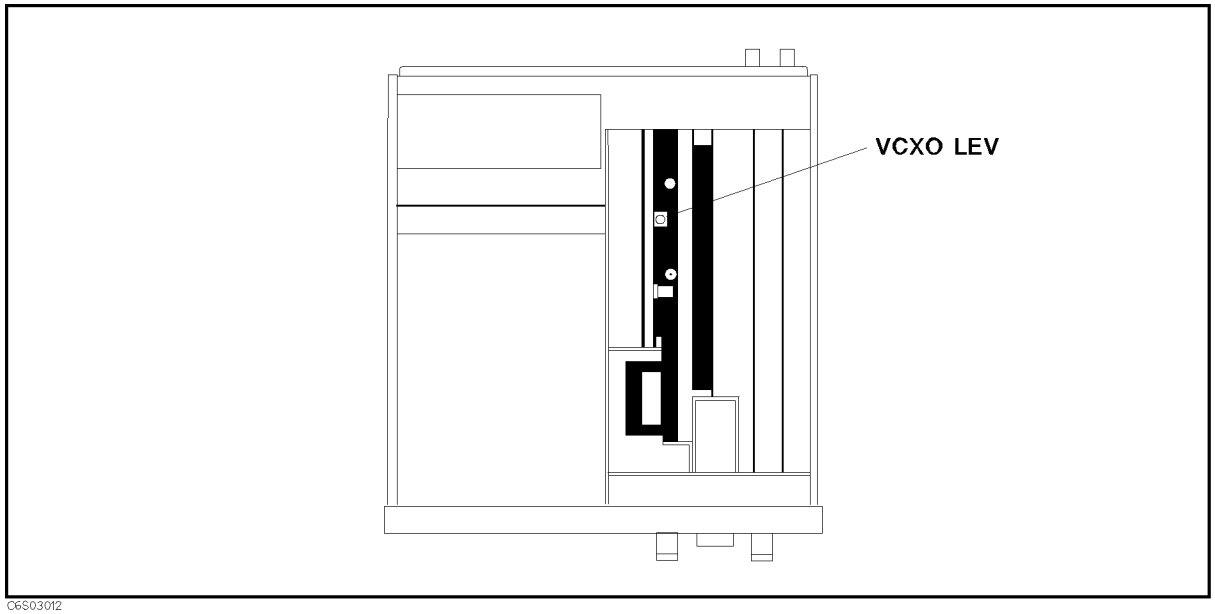


Figure 3-10. Source VCXO Adjustment Location

THIRD LOCAL VCXO ADJUSTMENT

The purpose of this procedure is to optimize the source VCXO oscillation.

Required Equipment

None

Procedure

1. Turn the HP 4286A OFF.
2. To gain access the adjustment component, remove the side panel on the control keys side.
3. Do not connect anything to the HP 4286A mainframe front terminals.
4. Press the following keys to execute adjustment test No.28:
   (PRESET), (SYSTEM), SERVICE MENU, TESTS, (2), (8), (x1), EXECUTE TEST
   The VCXO output level is displayed in the "R :" field.
5. Rotate "VCXO ADJ" and confirm that two voltage peaks appear in a rotation to confirm that the VCXO circuit is correct. Then press CONT.
6. Rotate "VCXO ADJ" slowly to enable instrument to memorize the peak voltage. Then press CONT.
7. Adjust "VCXO ADJ" until the VCXO level is within the limits and "PASS" is displayed. The limit is the memorized peak voltage +0/-1 %. Then press CONT to complete the adjustment.

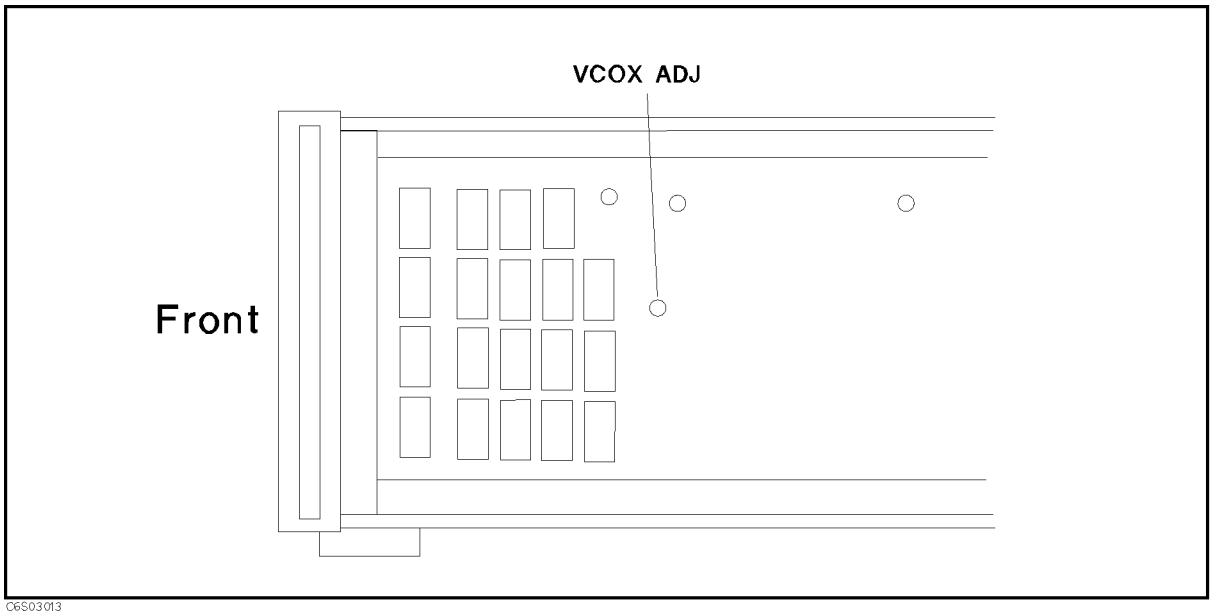


Figure 3-11. Third Local VCXO Adjustment Location

SOURCE MIXER LOCAL LEAKAGE ADJUSTMENT

The purpose of this procedure is to minimize the source mixer local leakage.

Required Equipment

Spectrum Analyzer ..... HP 8566A/B
N(m)-BNC(f) adapter (2 required) ..... PN 1250-1476
BNC cable, 122 cm (2 required) ..... PN 8120-1840

Procedure

1. Connect the equipment as shown in Figure 3-12.

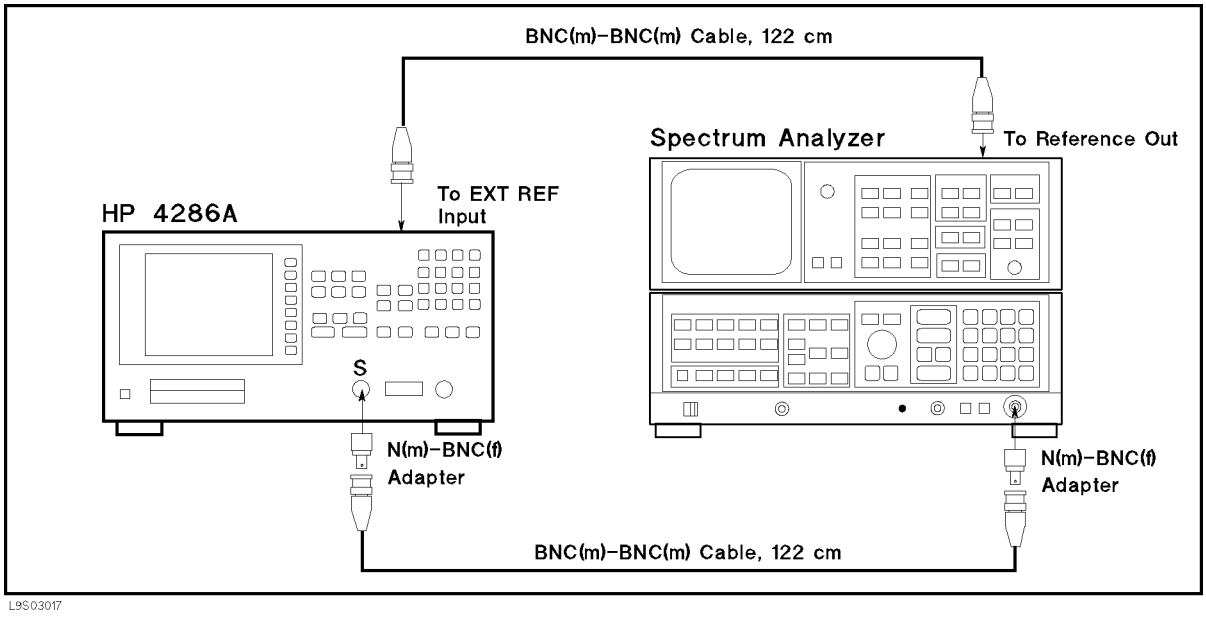


Figure 3-12. Source Mixer Local Leakage Adjustment Setup

2. Set the spectrum analyzer as follows:

Center Frequency	100 MHz
Span	100 MHz
RBW	300 kHz

3. Press the following keys to execute adjustment test No.30:

(PRESET), (SYSTEM), SERVICE MENU, TESTS, (3), (0), (x1), EXECUTE TEST

4. Adjust the local leakage adjustments until the spectrum analyzer reading at the 78.58 MHz signal level is less than −40 dBm. Then press CONT to complete the adjustment. The adjustment locations are shown in Figure 3-13.

Note

Carefully rotate the local leakage adjustments so that the adjustments are not misadjusted by much. It would be very difficult to recover from a large misadjustment.

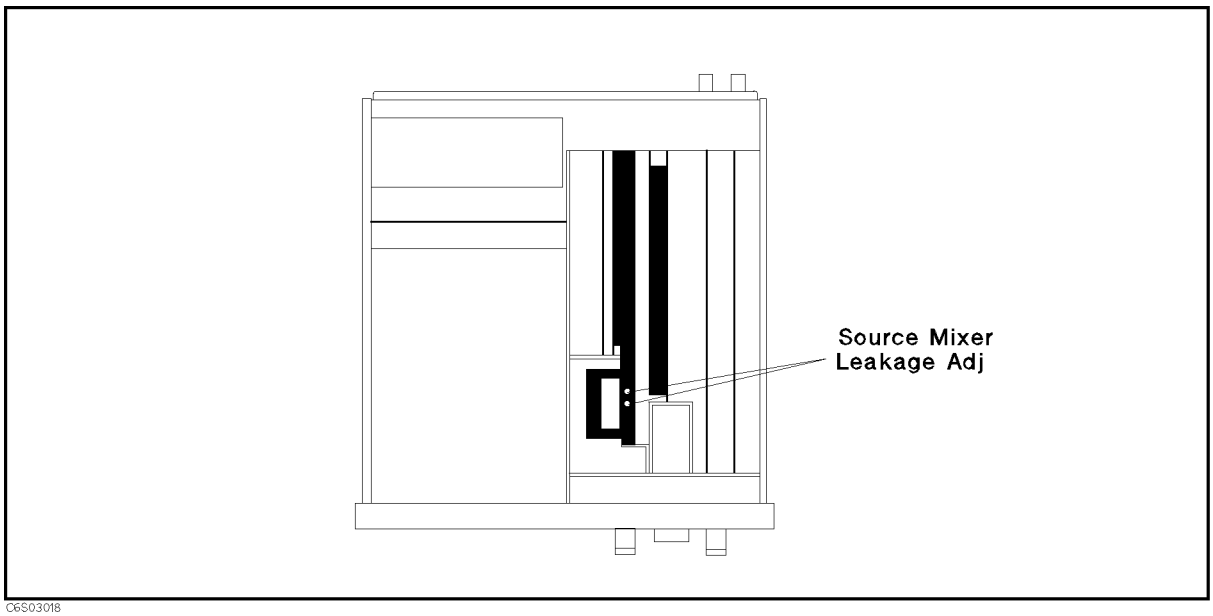


Figure 3-13. Source Mixer Leakage Adjustment Location

OSC LEVEL CORRECTION CONSTANTS

The purpose of this procedure is to obtain the correction constants that correct the OSC signal linearity and flatness.

Required Equipment

Power Meter	HP 436A
Power Sensor	HP 8482A
APC3.5-APC7 Adapter	PN 1250-1746[1]
APC3.5(m)-APC3.5(f) Right Angle Adapter	PN 1250-1249[2]
Test Fixture Stand	PN 04286-60141[1]

[1]: HP 4286A furnished accessory
[2]: HP 4286A option 021/022 furnished accessory

Procedure

1. Connect the HP 4286A and the computer with an HP-IB cable.
2. If the program "TE_A4286A" has not been performed for the equipment to be used, perform it (see the "Preparation for Using the Adjustment Program" paragraph).
3. Set the mass storage unit specifier (MSUS) to the address of the drive or the directory where the Adjustment Program "ADJ4286A" is located.
4. Load and run "ADJ4286A".
5. Choose "INITIAL SETUP" if you want to update the Calibrated Value for the power sensor.
6. Choose "OSC Level CC" for updating OSC Level Correction Constants. Follow the instructions on the controller's screen until the program ends. Figure 3-14 and Figure 3-15 show the equipment setup for the Correction Constants.

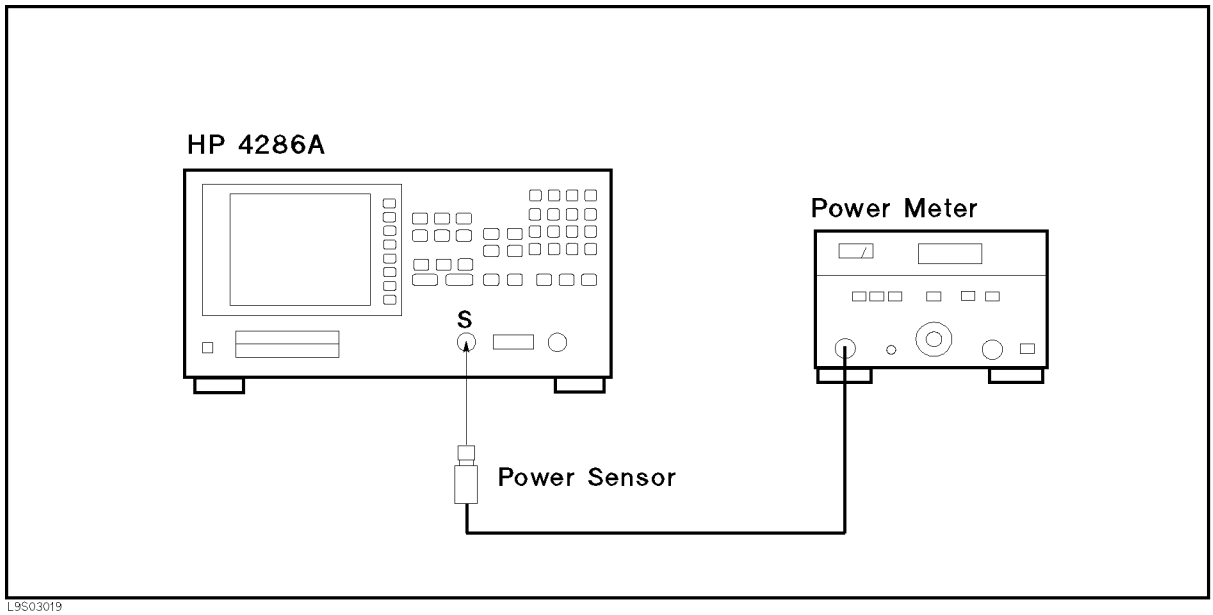


Figure 3-14. OSC Level Correction Constants Setup (1)

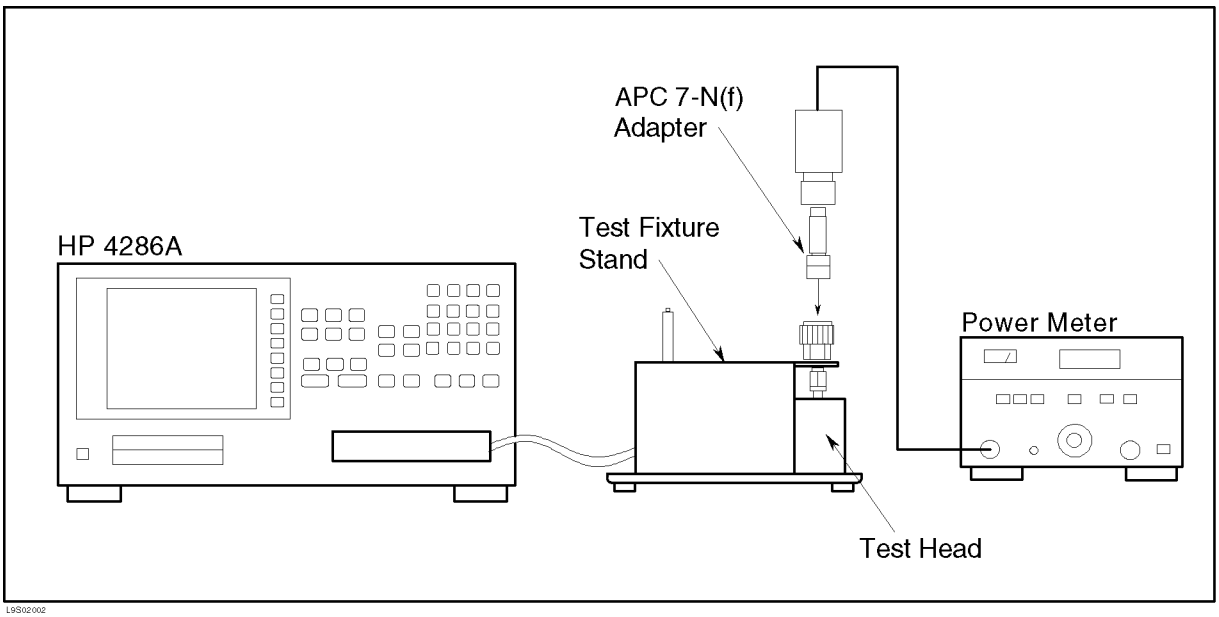


Figure 3-15. OSC Level Correction Constants Setup (2)

HOLD STEP ADJUSTMENT

The purpose of this procedure is to minimize the hold step level of the A6 receiver sample hold output.

Required Equipment

None

Procedure

1. Turn the HP 4286A OFF.
2. To gain access the adjustment component, remove the side panel on the control keys side.
3. Do not connect anything to the HP 4286A mainframe front terminals.
4. Turn the HP 4286A ON.
5. Press the following keys to execute adjustment test No.26:
   (PRESET), (SYSTEM), SERVICE MENU, TESTS, (2), (6), (x1), EXECUTE TEST
   The hold step level is displayed in the "R :" field.
6. Adjust "HOLD STEP ADJ" until the hold step level is within 0 ± 200 mU and "PASS" is displayed. Then press CONT to complete the adjustment. The adjustment location is shown in Figure 3-16.

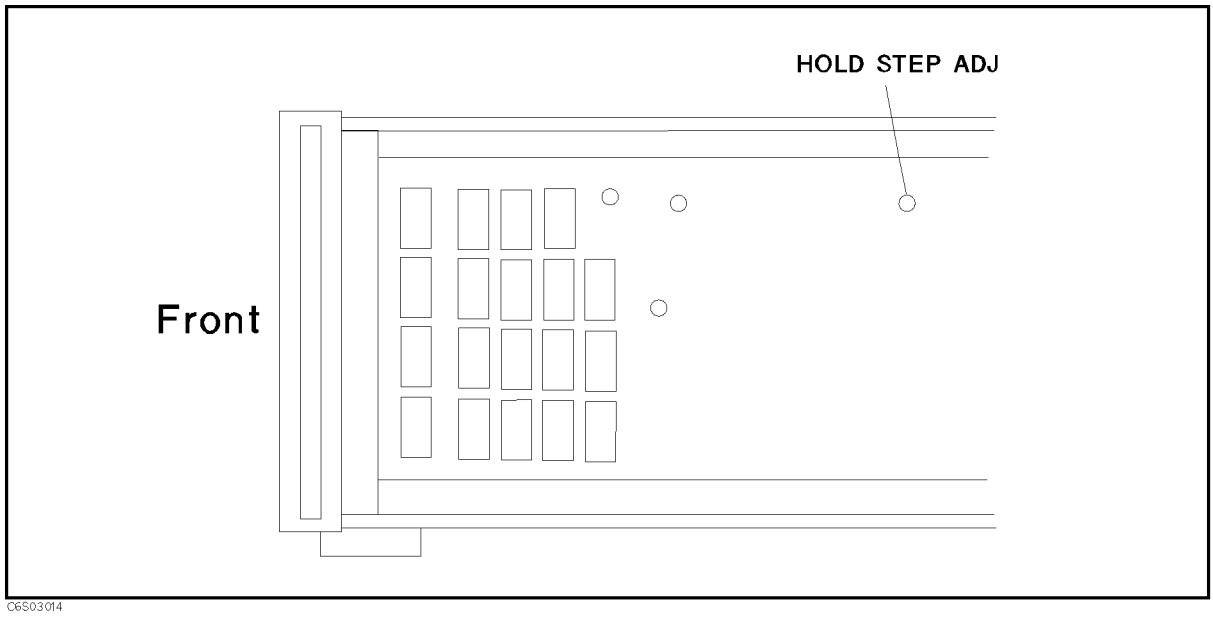


Figure 3-16. Hold Step Adjustment Location

BAND PASS FILTER ADJUSTMENT

The purpose of this procedure is to optimize the A6 receiver IF band pass filter.

Required Equipment

Type-N Cable, 61 cm .....HP 11500B or part of HP 11851B

Procedure

1. Turn the HP 4286A OFF.
2. To gain access the adjustment component, remove the side panel on the control keys side.
3. Connect the equipment as shown in Figure 3-17.

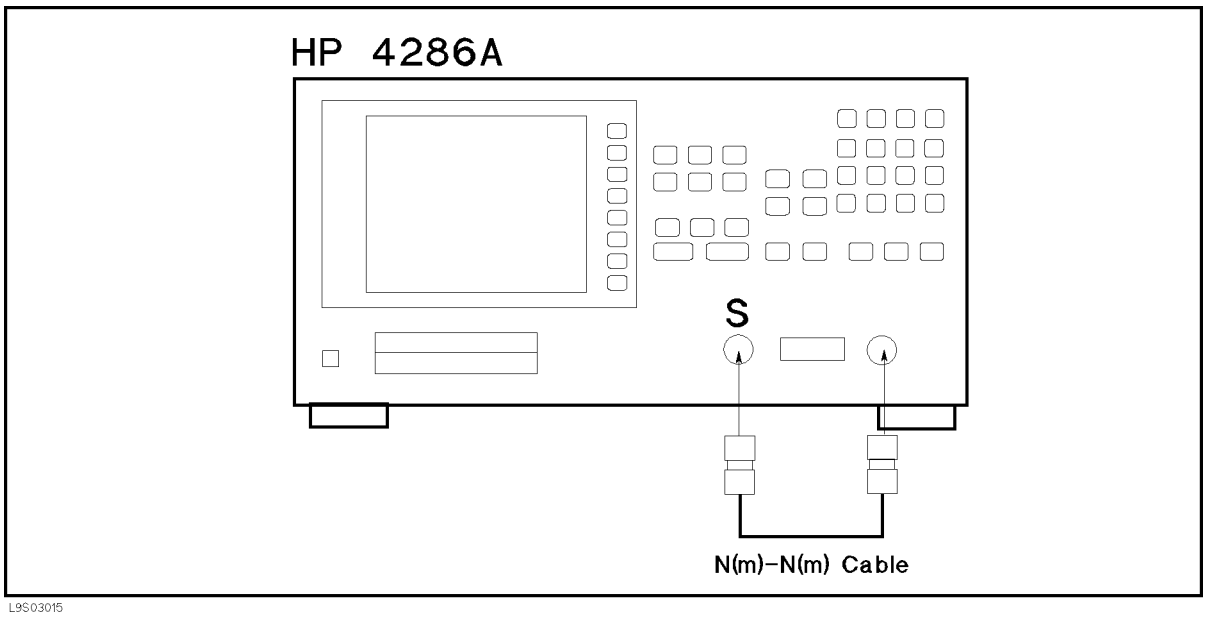


Figure 3-17. Band Pass Filter Adjustment Setup

4. Turn the HP 4286A ON.
5. Press the following keys to execute adjustment test No.27:
   (PRESET), (SYSTEM), SERVICE MENU, TESTS, (2), (7), (x1), EXECUTE TEST The receiver gain monitor value is displayed in the "|Z| :" field.
6. Adjust "BPF ADJ 1" to maximize the monitor value. Then adjust "BPF ADJ 2" to maximize the monitor value and press CONT to complete the adjustment. The adjustment location is shown in Figure 3-18. (The interaction of "BPF ADJ1" and "BPF ADJ 2" is negligible.)

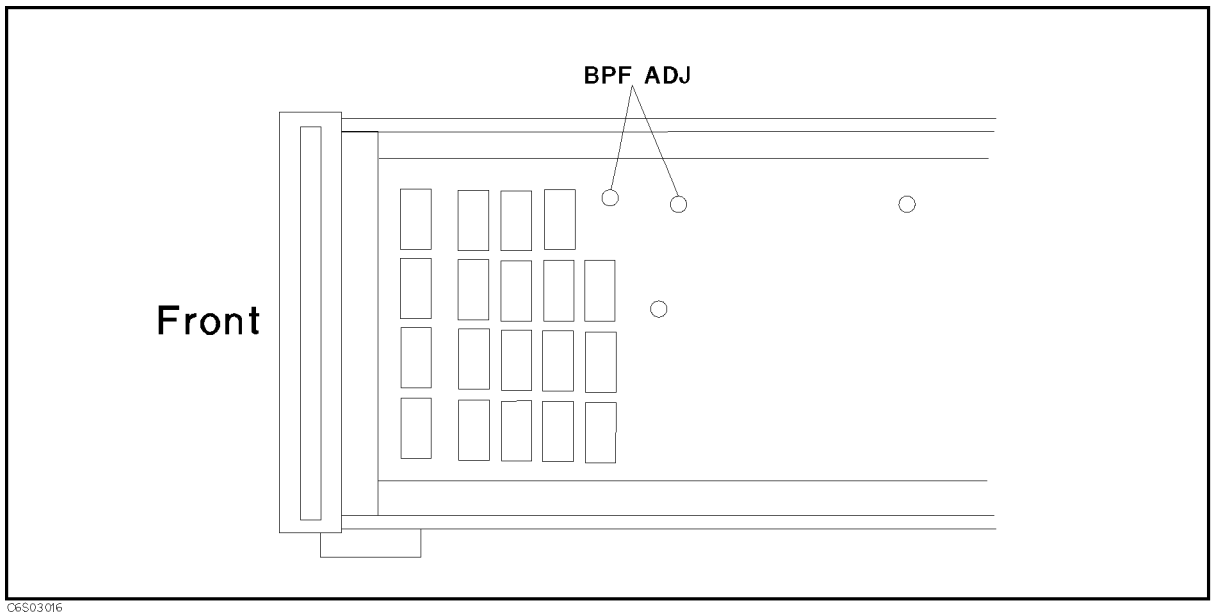


Figure 3-18. Band Pass Filter Adjustment Location

Display Adjustment

The purpose of this procedure is to adjust the CRT display.

Note The display adjustments are optional and normally the CRT does not require adjustment. You should use this procedure only when the display is obviously out of adjustment.

Test Equipment

Digital Multimeter	HP 3456A, HP 3457A or HP 3458A
Dual Banana Plug to Alligator Clip Lead	HP 11002A

Procedure

Warning **Dangerous voltage levels exist in this CRT unit and can result in serious personal injury or death if you come into contact with them.**

1. Turn HP 4286A OFF.
2. Remove CRT unit from the unit according to the CRT Assembly Removal section in the Replacement Procedures chapter.
3. Remove the top cover of the CRT unit by unscrewing six screws.
4. Connect the Dual Banana Plug to Alligator Clip Lead to the Multimeter.
5. Connect the high lead to the end of R901 closest to the fuse, and low lead to the HP 4286A chassis. The component is shown in Figure 3-19.

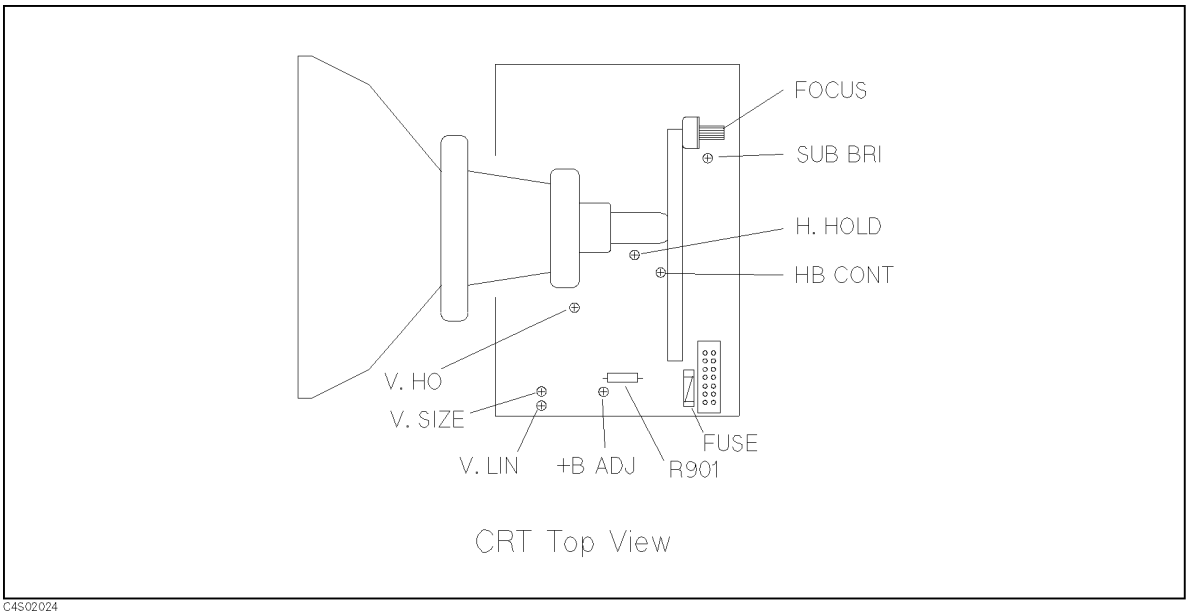


Figure 3-19. CRT Adjustment Location

6. Turn HP 4286A ON.
7. Adjust +B ADJ until the digital multimeter reading is +14.00 V.
8. Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (3), (3), (x1), EXECUTE TEST, CONT to display the Test Pattern.
9. Adjust V.HO (vertical hold) for vertical synchronization.
10. Adjust Focus for the best focus.
11. Adjust V.Lin (vertical linearity) until the grid pattern crosses at right angles.
12. Press softkey 8 (the bottom softkey) to exit the test pattern.
13. Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (3), (2), (x1), EXECUTE TEST, CONT to display the Test Pattern.
14. Adjust V.Size (vertical size) until the vertical length of the rectangle is approximately 100 mm.
15. Adjust H.Hold (horizontal hold) to center the display horizontally.
16. Press softkey 8 (the bottom softkey) to exit the test pattern.

4

Overall Troubleshooting

This chapter consists of the following sections:

- Troubleshooting Summary
- Inspecting the Power On Sequence
- Verifying Functional Groups
- Troubleshooting the HP-IB System

The *Troubleshooting Summary* outlines how to troubleshoot the HP 4286A using the troubleshooting flow diagram.

Inspecting the Power ON Sequence begins the troubleshooting procedures by inspecting the power on sequence.

Verifying Functional Groups provides verification procedures to isolate the problem to the faulty functional group.

Troubleshooting the HP-IB System gives some hints for troubleshooting when the HP 4286A is used in an HP-IB system.

TROUBLESHOOTING SUMMARY

The troubleshooting strategy of this manual is based on a verification (rather than symptomatic) approach. Verification procedures and the resulting corrective actions are given in the manual. By following these directions, you will determine the faulty assembly that must be replaced.

Figure 4-1 shows the overall troubleshooting flow. The following paragraphs provide brief descriptions of the troubleshooting sequence:

Troubleshooting is started by performing the Inspect Power On Sequence.

Inspecting the power on sequence and verifying faulty groups may indicate one or more faulty groups in the HP 4286A's five functional groups. (The HP 4286A can be divided into five functional groups: power supply, digital control, source, receiver, and transducer.)

A faulty assembly is isolated to a faulty functional group according to the troubleshooting procedure for each faulty group. The troubleshooting procedures are given in Chapters 5 to 9.

A faulty assembly is replaced according to Chapters 12 and 13. Chapter 12 lists the replaceable parts and Chapter 13 provides replacement procedures for the major parts.

The procedures required after an assembly replacement, such as adjustments and performance tests, are given in Chapter 14.

Troubleshooting hints that can be used when the HP 4286A is used in an HP-IB system are given in this chapter. When the HP 4286A is used in an HP-IB system, the HP 4286A's HP-IB function needs to be verified as the first step in troubleshooting.

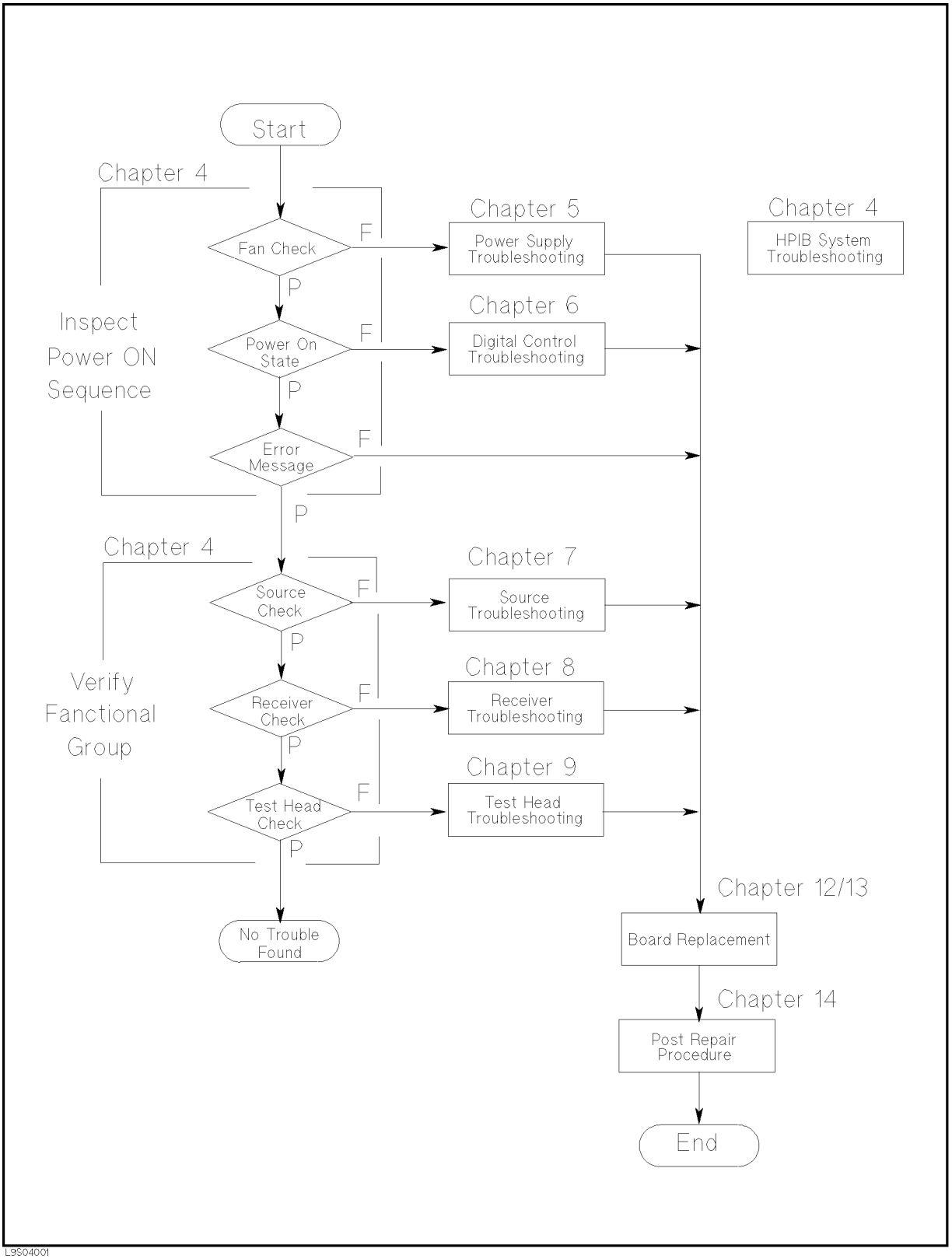


Figure 4-1. Overall Troubleshooting Flow

INSPECTING THE POWER ON SEQUENCE

This section begins the troubleshooting procedures by inspecting the power on sequence.

Check the Fan

Turn the HP 4286A power on. Inspect the fan on the rear panel.

- The fan should be rotating and audible.

In case of unexpected results, check the AC line power to the HP 4286A. Check the fuse (the rating is listed on the rear panel). Check the line voltage setting. To set the line voltage, see the *Power Requirements* in Appendix C.

If the problem persists, continue with Chapter 5.

Check the Power On State

Turn on the HP 4286A and verify for the following events in the listed order:

1. Beep sounds in a about second.
2. The display comes up bright and focused.

In case of unexpected results, continue with Chapter 6.

Check Error Message

Turn the HP 4286A power on, and inspect the display. No error message should be displayed. If one of the error messages listed below is displayed, follow the instructions described below. For any other message, see the *Error Messages* in Messages.

Error Messages	**Instruction**
`POWER ON TEST FAILED`	This indicates the power on self-test failed. Continue with*Troubleshooting When Power On Self-test Failed*
`EEPROM CHECK SUM ERROR`	This indicates that the correction constants stored in the EEPROM on the A1 CPU are invalid or the EEPROM is faulty. Continue with Chapter 6.
`Svc` (Status Annotation)	This indicates that the correction constants stored in the EEPROM on the A1 CPU are invalid or the EEPROM is faulty. Continue with Chapter 6.
`POWER FAILED ON - - -`	One or more of the A2 power supplies (+65 V, +15 V, +8.5 V, +5.3 V, +5 V, -5 V, -15 V) is displayed in - - - of the message. The displayed power supplies are shutdown due to trouble in the A2 post-regulator. Continue with Chapter 5.
`POWER FAILED ON PostRegHot`	This indicates the A2 power supplies (+15 V, +8.5 V, +5.3 V, +5 V, -5 V, -15 V) are shutdown because the heat sink on the A2 post-regulator is too hot. Cool down the HP 4286A for about 30 minutes. Then turn the HP 4286A power on. If this message is still displayed, replace the A2 post-regulator.
`PHASE LOCK LOOP UNLOCKED`	This indicates one or more of PLLs (phase lock loops) in the oscillators is not working properly. Continue next with *Troubleshooting When Power On Self Test Failed* .

Troubleshooting When Power On Self-Test Failed

Note

The HP 4286A performs the power on self-test every time the HP 4286A is turned on. In the power on self-test, internal diagnostic tests 1, 4, 5, 6, 7, and 8 through 15 are executed sequentially. The first failed test indicates the most probable faulty assembly. For more information about the internal tests, see Chapter 10.

If the power on self-test fails and the "POWER ON TEST FAILED" message is displayed, execute the ALL INT test, using to the following procedure, to identify the first failed test. Then replace the probable faulty assembly (see the Table 4-1).

a. Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (0), and (x1) to access internal test 0: ALL INT.
b. Press EXECUTE TEST to execute the ALL INT test.
c. Wait until the test result (PASS or FAIL) is displayed.
d. Press the (↑), (↓) keys to find the first occurrence of a FAIL message for test 1 and tests 4 through 14.

Table 4-1. Troubleshooting Information for Internal Test Failure

Test No.	First Failed Test	Troubleshooting Information
1	A1 CPU	Replace A1 CPU.[1]
4	A2 POST REGULATOR	Continue with the next *A2 POST REGULATOR Test Fail* section.
5	A6 A/D CONVERTER	The A6 receiver IF is the most probable faulty board. Replace the A6 receiver IF.
6	A5 REFERENCE OSC	The A5 synthesizer is the most probable faulty board. Replace the A5 synthesizer.
7	A5 FRACTIONAL N	The A5 synthesizer is the most probable faulty board. Replace the A5 synthesizer.
8	A4A1 1ST LO OSC	The A4A1 1st LO OSC is the most probable faulty board. Replace the A4 1st LO/Receiver RF.
9	A3A2 2ND LO OSC	The A3A2 2nd LO OSC is the most probable faulty board. Replace the A3A2 2nd LO.
10	A3A1 DIVIDER	The A3A1 Source Vernier is the most probable faulty board. Replace the A3A1 Source Vernier.
11	A6 3RD LO OSC	The A6 receiver IF is the most probable faulty board. Replace the A6 receiver IF.
12	A3A1 SOURCE OSC	The A3A1 Source Vernier is the most probable faulty board. Replace the A3A1 Source Vernier.
13	A6 SEQUENCER	The A6 receiver IF is the most probable board. Replace the A6 receiver IF.
14	SOURCE LEVEL	Continue with Chapter 7.

1 EEPROM with data needs to be replaced, see Chapter 13.

A2 POST REGULATOR Test Fail

If internal test 4: A2 POST REGULATOR is the first failed test, the power supply functional group is the most probable faulty group. See Chapter 5.

Also, the test failure might be caused by A6 A/D converter trouble. Execute internal test 5: A6 A/D CONVERTER to verify the A/D converter, with the following procedure. If the test 5 fails, suspect the A5 synthesizer and A6 receiver IF in addition to the power supply functional group.

i. Press (5), (x1), EXECUTE TEST to execute internal test 5: A6 A/D CONVERTER.
ii. Wait until the test result (PASS or FAIL) is displayed.

VERIFYING FUNCTIONAL GROUPS

This section provides procedures to isolate the faulty group.

Source Verification

Verify source group operation using the following procedure:

Test Equipment

Frequency Counter	HP 5343A Option 001
Power meter	HP 436A Opt. 022, HP 437B, or HP 438A
Power Sensor	HP 8482A
BNC cable, 61 cm	PN 8120-1839
N(m)-BNC(f) adapter	PN 1250-1476

Procedure

1. Perform the frequency accuracy test (see Chapter 2).
   - If the test fails, go to Chapter 7.
2. Calibrate the power meter for the power sensor.
3. Connect the equipment as shown in Figure 4-2.

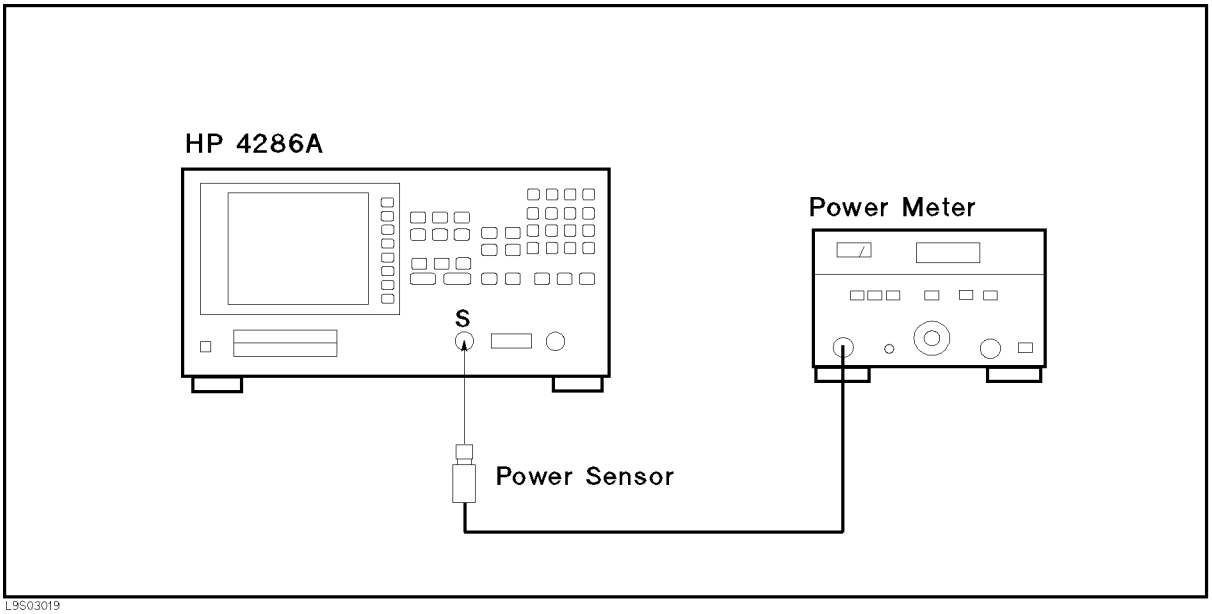


Figure 4-2. Source Test Setup

4. Turn the HP 4286A power on.
5. Press (SYSTEM), SERVICE MENU, SERVICE MODES, CORRECTION CONSTANTS, OSC LVL CC, FRONT to select the source correction constants for the front output connector.
6. Press (Source), OSC UNIT, dBm, (−), (1), (9), (x1) to set the osc level to −19 dBm.
7. Perform the test for all settings listed in Table 4-2. Confirm that each power meter reading is within the test limits shown in the table.

Table 4-2. Source Test Settings

Frequency	Osc Level	Test Limit
1 MHz	−19 dBm	± 2 dB
10 MHz	−13 dBm	± 2 dB
100 MHz	−7 dBm	± 2 dB
1 GHz	7 dBm	± 2 dB

- If the test fails, perform the OSC level correction constants according to Chapter 3. If the test still fails, go to Chapter 7.
- If the test passes, continue with the next step.

8. Press (Preset), and the HP 4286A test frequency is set to 1 GHz.
9. Press (SYSTEM), SERVICE MENU, SERVICE MODES, OSC, OSC AUTO man, {then the label changes to OSC auto MAN} to set the HP 4286A manual OSC level mode.
10. Press OUTPUT ATT [AUTO], 10 dB (and verify the label changes to OUTPUT ATT [10 dB]) to set the output attenuator to 10 dB.

11. Press `OSC DAC AUTO man` (and verify the label changes to `OSC DAC auto MAN`), `OSC DAC VALUE`, 3, 2, 0, 0, 0, x1 to set the DAC value to 32,000.

12. Confirm that the power meter reading is greater than 6.5 dBm.

    - If the test fails, go to Chapter 7.
    - If the test passes, continue with the next *Receiver Test* procedure.

Receiver Verification

Verify the receiver operation using the following procedure.

Test Equipment

Type-N Cable, 61 cm .....HP 11500B or part of HP 11851B

Procedure

1. Verify that nothing is connected to the front panel of the HP 4286A mainframe.
2. Turn the HP 4286A power on.
3. Press (PRESET) to initialize the HP 4286A.
4. Press (SYSTEM), SERVICE MENU, TESTS, (2), (0), (x1) to access the RECEIVER GAIN test. When "RECEIVER GAIN" is displayed, press EXECUTE TEST.
5. Perform the test according to the displayed instructions.
   - If the test fails, go to Chapter 8.
6. Press (↑) to access the A6 V/I NORMALIZER test. When "A6 VI NORMALIZER" is displayed, press EXECUTE TEST.
7. Perform the test according to the displayed instructions.
   - If the test fails, replace A6 receiver IF.
8. Press (↑) to access the FRONT ISOL'N test. When "FRONT ISOL'N" is displayed, press EXECUTE TEST.
9. Perform the test according to the displayed instructions.
   - If the test fails, go to Chapter 8. If the test passes, continue with the next *Transducer Test* procedure.

Test Head Verification

Verify the test head operation using the following procedure.

Test Equipment

APC7 Calibration Kit ..... HP 4286A furnished accessory
N(m)-N(m) cable

Procedure

1. Turn the HP 4286A power on.
2. Press (SYSTEM), SERVICE MENU, TESTS, (2), (4), (x1) to access the TEST HEAD diagnostic test.
3. Press EXECUTE TEST to perform the test. The test procedure is as follows:

   a. Connect the HP 4286A S and R connectors with the N(m)-N(m) cable, and press CONT. The HP 4286A mainframe is calibrated for the test.

   b. Connect the test head to the mainframe, and connect the APC3.5(m)-APC7 adapter to the test head using the test fixture stand as shown in Figure 4-3.

   c. Connect the open termination of the APC7 calibration kit to the test head, and press CONT. The open test is performed.

   d. In the same manner, perform the short and 50 Ω tests with the short and 50 Ω terminations of the APC7 calibration kit, following the displayed instructions.

- If the test fails, go to Chapter 9.
- If the test passes, the HP 4286A is probably operating correctly

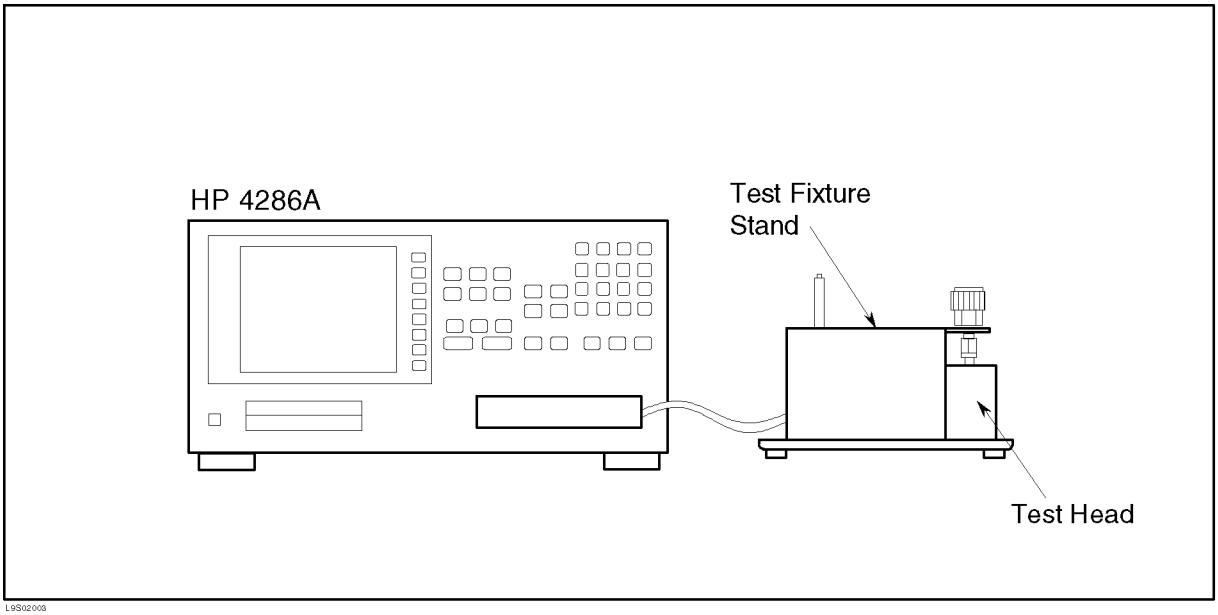


Figure 4-3. Test Head Diagnostic Test Setup

TROUBLESHOOTING HP-IB SYSTEM

Check the HP 4286A's HP-IB functions with a known working passive peripheral (like a plotter or printer).

1. Connect the peripheral using a good HP-IB cable to the HP 4286A. Turn the HP 4286A power on.
2. Press (Local), `SYSTEM CONTROLLER`. Then press `SET ADDRESSES` and press `ADDRESS: PLOTTER` or `ADDRESS PRINTER` to see the peripheral addresses recognized by the HP 4286A. The factory default addresses are:

Table 4-3. Default HP-IB Addresses

DEVICE	HP-IB ADDRESS
Plotter	5
Printer	1

3. Set the HP-IB address of the peripheral to the address that the HP 4286A recognizes. Peripheral addresses are often set with a rear panel switch. See the applicable peripheral manual to read or change its address.
4. Turn the peripheral power on.
5. Press (COPY), and `PLOT` or `PRINT [STANDARD]`. A copy of the display should plot or print out.
   - If the result is a copy of the display, the HP-IB function is working in the HP 4286A.
   - If the result is not a copy of the display, suspect HP-IB problems in the HP 4286A. Continue with Chapter 6.

Check the External Controller

If unexpected operations occur when controlling the HP 4286A with an external controller, perform the following checks to verify the problem is not with the controller.

- Check compatibility (it must be HP 9000 series 200/300). See the controller and the BASIC system manuals.
- The HP-IB interface hardware must be installed in the controller. See the controller and the BASIC system manuals.
- The I/O and HP-IB binaries must be loaded. See the BASIC system manuals.
- Check the select code. See the BASIC system manuals.
- Check the HP-IB cables. See the BASIC system manuals.
- Check the programming syntax. See the BASIC system manuals.

If the HP 4286A is still operating incorrectly after these checks are verified, continue with Chapter 6.

5

Power Supply Troubleshooting

INTRODUCTION

Use this procedure only if you have read Chapter 4 and you believe the problem is in the power supply. The procedure is designed to let you identify the bad assembly within the power supply functional group in the shortest possible time.

The power supply functional group consists of:

- A40 Pre-Regulator
- A2 Post-Regulator
- A52 DC-DC Converter

All assemblies, however, are related to the power supply functional group because power is supplied to each assembly. Figure 5-1 shows all power lines in simplified block diagram form. For more information about the signal paths and specific connector pin numbers, see Figure 5-13, Figure 5-14, and Figure 5-15 at the end of this chapter.

If an assembly is replaced, see Chaptre 14. It tells what additional tests or adjustments need to be done after replacing any assembly.

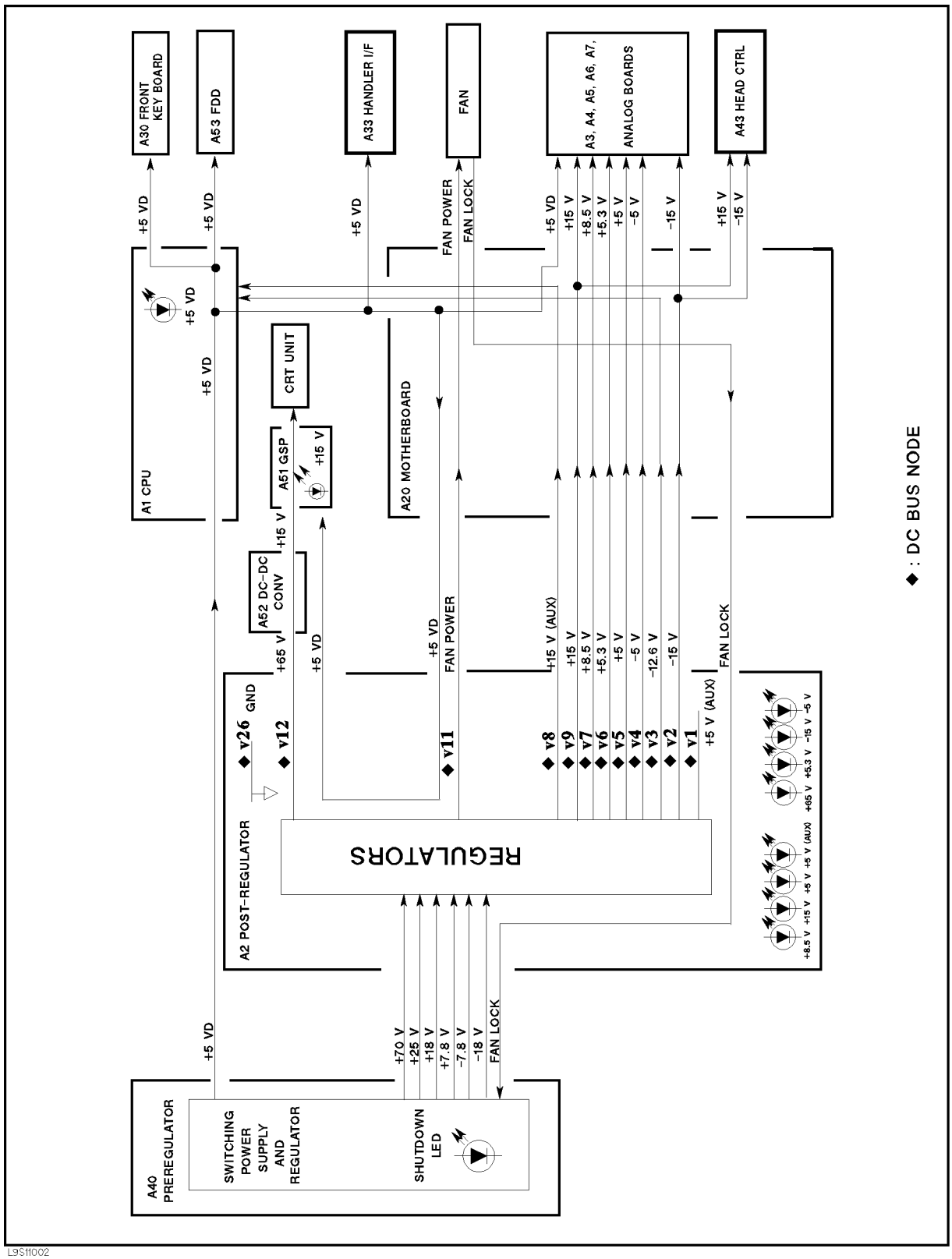


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Figure 5-1. Power Supply Lines Simplified Block Diagram

POWER SUPPLY TROUBLESHOOTING SUMMARY

This summary gives an overview of the power supply troubleshooting procedure. Technicians who are already familiar with troubleshooting the power supply may save time by following this summary instead of reading the entire procedure. Headings in this summary match the headings in the procedure.

Start Here

1. Check Error Messages
   If one of the error messages listed below is displayed, continue with the *TROUBLESHOOT THE A2 POST-REGULATOR.*
   ```
   POWER FAILED ON - - -
   POWER FAILED ON PostRegHot
   ```
2. Check the Fan is Rotating
   If the fan is not rotating, continue with the *FIND OUT WHY THE FAN IS NOT ROTATING.*
3. Check the A40 SHUTDOWN LED
   If the A40 SHUTDOWN LED is on, continue with the *FIND OUT WHY THE A40 SHUTDOWN LED IS ON.*
4. Check the A1 +5 VD LED
   If the A1 +5 VD LED is not on, continue with the *FIND OUT WHY THE +5 VD LED IS NOT ON STEADILY.*
5. Check the A2 Eight LEDs
   If one or some of the A2 eight LEDs are off, continue with the *TROUBLESHOOT THE A2 POST-REGULATOR.*
6. Run the Internal Test 4: A2 POST REGULATOR
   If the internal test 4 fails, continue with the *TROUBLESHOOT THE A2 POST-REGULATOR.*

Find Out Why the Fan is Not Rotating

1. Check the Line Voltage, Selector Switch Setting, and Fuse
2. Check the A40 SHUTDOWN LED

Find Out Why The A40 SHUTDWON LED is On

1. Disconnect the Cable from the A40J1
2. Disconnect the Cable from the A51J2
3. Disconnect the Cable from the A1J10
4. Remove Assemblies

Find Out Why the +5 VD LED is Not On Steadily

1. Check the A40 Pre-Regulator
2. Disconnect Cables on the A1 CPU
3. Remove Assemblies

Troubleshoot the Fan and the A40 Pre-Regulator

1. Troubleshoot the Fan
2. Troubleshoot the A40 Pre-Regulator

Troubleshoot the A2 Post-Regulator

1. Check the A40 Pre-Regulator
2. Remove Assemblies
3. Measure the A2 Post-Regulator Output Voltages

Troubleshoot the A52 DC-DC Converter

1. Disconnect Flat Cables from A52J1 and A52J3.
2. Check the A52 TP4 voltage.

START HERE

1. Check Error Messages

Turn the HP 4286A power on. If one of error messages listed below appears on the display, follow the instruction of the displayed error message. If no error message is displayed, continue with the next *Check the Fan is Rotating.*

Error Messages	Instruction
`POWER FAILED ON - - -`	One or some of A2 power supplies, +65 V, +15 V, +8.5V, +5.3 V, +5 V, -5 V, -15 V are displayed in - - - of the message. The displayed power supplies are shut down due to the trouble on the A2 post-regulator. Continue with the *CHECK THE A2 EIGHT LEDs* in this *START HERE.*
`POWER FAILED ON PostRegHot`	This indicates A2 power supplies, +15 V, +8.5 V, +5.3 V, +5 V, -5 V, -15 V, are shut down due to too hot heat sink on A2 post-regulator. Cool down the HP 4286A for about 30 minutes. Then turn the HP 4286A power on. If this message is still displayed, replace A2 post-regulator.

These messages are associated with the power supplies functional group. These messages indicate the A2 protective shutdown circuit is shutting down some of A2 power supplies to protect them from over current, over voltage, under voltage, and too hot conditions. For more information about the A2 shutdown circuit, see the Figure 5-14 Power Supply Block Diagram 2.

Note

These messages are displayed only after the power on sequence. When one of these message is displayed, the HP 4286A's front keys are disabled. In the power on sequence, the HP 4286A checks the shutdown status of the A2 power supplies, +65 V, +15 V, +5 V, -5 V, -15 V. If a power supply is shut down, the HP 4286A displays an error message and stops its operation. Once the HP 4286A stops the operation, any front key operations are disabled. The only way to reset the HP 4286A is turning the HP 4286A power off.

2. Check the Fan is Rotating

Look at the fan on the rear panel. Check the fan is rotating.

- If the fan is not rotating, continue with the *FIND OUT WHY THE FAN IS NOT ROTATING* in this chapter.
- If the fan is rotating, continue with the next *Check the A40 SHUTDOWN LED.*

3. Check the A40 SHUTDOWN LED

There is a LED, SHUTDOWN LED, on the A40 pre-regulator. Perform the following procedure to check it. The SHUTDOWN LED is described in the next *A40 SHUTDOWN LED* .

a. Turn the HP 4286A power off.

b. Remove the HP 4286A top cover and shield plate.

c. Turn the HP 4286A power on.

d. Look at the A40 SHUTDOWN LED. The LED is normally off. The SHUTDOWN LED location on A40 pre-regulator is shown in Figure 5-2.

- If the A40 SHUTDOWN LED is on, check the cable connection between A40J2 and A2J4. If the connection is good, continue with the *FIND OUT WHY THE A40 SHUTDOWN LED IS ON* in this chapter.
- If the A40 SHUTDOWN LED is off, continue with the *Check the A1 +5 VD LED* in this procedure.

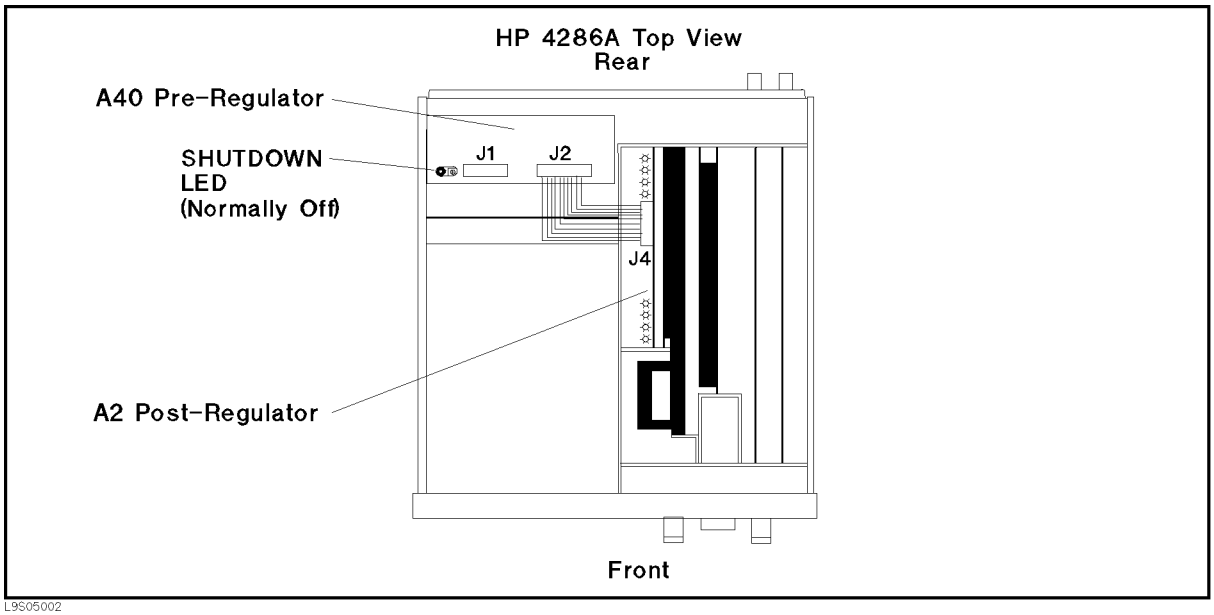

Figure 5-2. A40 SHUTDOWN LED Location

A40 Shutdown LED

The A40 SHUTDOWN LED turning on indicates some of A40 power supply is shut down by the A40 shutdown circuitry.

There are two FAN conditions, rotating and not rotating when the SHUTDOWN LED turns on.

When the fan is not rotating, the shutdown circuit is probably activated by the over voltage condition on the +70 V power line or the FAN LOCK signal missing. In this condition, all A40 power supplies, +70 V, +25 V, +5 VD, +18 V, +7.8 V, -7.8 V, and -18 V are shut down.

When the fan is rotating, the shutdown circuit is probably activated by the over voltage condition on the +5 VD power line. In this condition, the A40 power supplies, +5 VD, +18 V, +7.8 V, -7.8 V, and -18 V are shut down.

For more information about the A40 shutdown circuit operation, see the Figure 5-13 Power Supply Block Diagram 1.

Note

Once the A40 shutdown circuit is activated, the only way to reset the circuit is turning the HP 4286A power off. Wait a minute after turning the HP 4286A off. Then turn it on.

4. Check the A1 +5 VD LED

a. Remove the HP 4286A's bottom cover.

b. Turn the HP 4286A power on.

c. Look at the +5 VD LED. The +5 VD LED location on A1 CPU is shown in Figure 5-3. The LED is normally on.

- If the +5 VD LED is off, continue with the *TROUBLESHOOT +5 VD POWER SUPPLY* in this chapter.
- If the +5 VD LED is on, the +5 VD power supply is verified with 95% confidence level. Continue with the *Check A2 Eight LEDs* in this procedure. If you want to confirm the last 5% uncertainty, perform steps in the next *Measure the A1 +5 VD Voltage*.

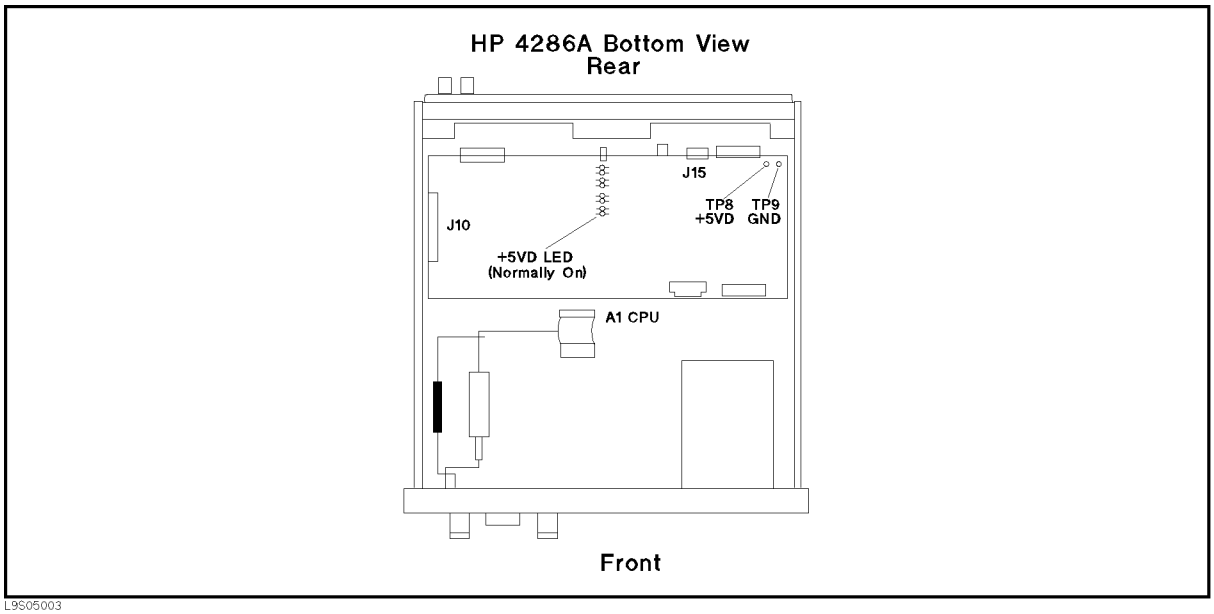

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Figure 5-3. A1 +5 VD LED Location

Measure the A1 +5 VD Voltage

Measure the DC voltage on a test point A1TP8 (+5 VD) using a voltmeter. Check the voltmeter reading is within 4.59 V to 5.61 V.

- If the voltmeter reading is out of the limits, continue with the *FIND OUT WHY THE A1 LED IS NOT ON STEADILY*.
- If the voltmeter reading is within the limits, continue with the next step.

5. Check the A2 Eight LEDs

a. Remove the HP 4286A's top cover and shield.

b. Turn the HP 4286A power on.

c. Look at the all A2 eight LEDs. The A2 LED locations are shown in Figure 5-4. The all LEDs are normally on.

- If one or some of the LEDs are off, continue with the *TROUBLESHOOT A2 POST-REGULATOR* in this chapter.

- If the all LEDs are on, continue with the next *Run the Internal Test 4: A2 POST REGULATOR*.

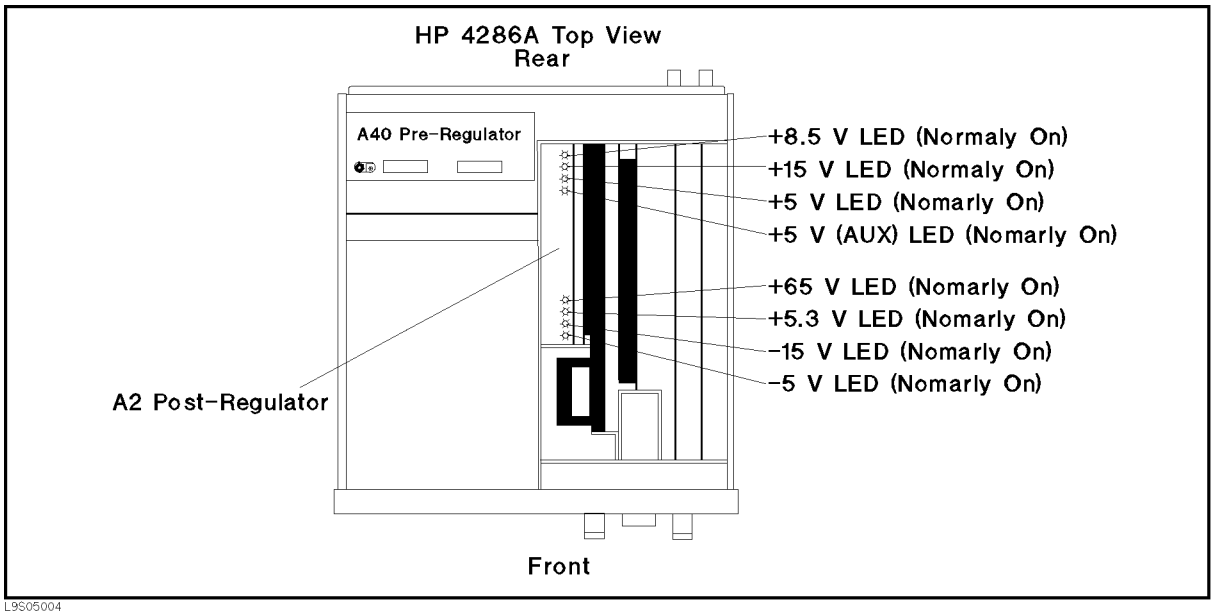

Figure 5-4. A2 Eight LED Locations

6. Run the Internal Test 4: A2 POST REGULATOR

The internal test 4: A2 POST REGULATOR verifies the A2 post-regulator. Perform the following procedure to check the A2 post-regulator. The internal test 4 is described in the next *Internal Test 4: A2 POST REGULATOR*.

Press (System), SERVICE MENU, TESTS, (4), (x1), EXECUTE TEST to execute the internal test 4: A2 POST REGULATOR. After the test completed, the test result is displayed as shown in Figure 5-5.

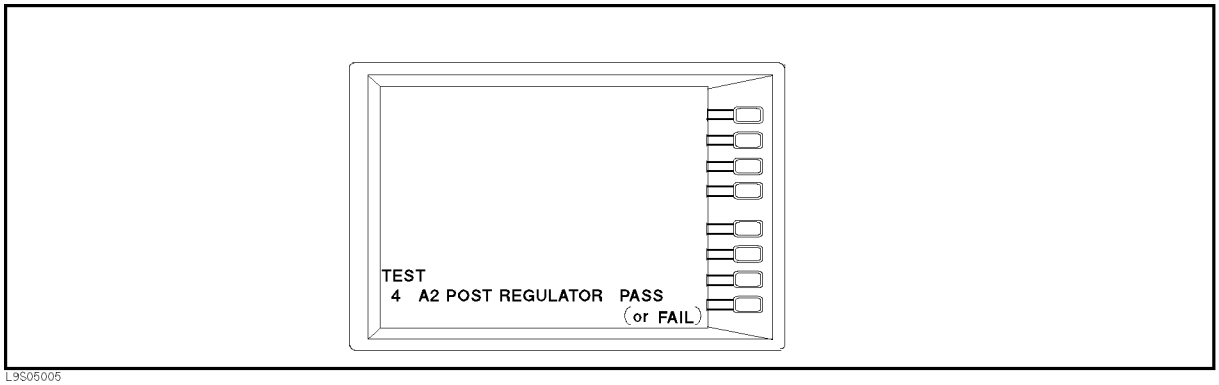

Figure 5-5. Displayed Test Result

- If "PASS" is displayed, the power supply function group are working properly with a 95% confidence level. To confirm the last 5% uncertainty of the A2 power supplies, measure the all A2 power supply voltages. See the *MEASURE A2 POST-REGULATOR OUTPUT VOLTAGE* at the end of this chapter.
- If "FAIL" is displayed, perform the following steps.

a. Press RETURN , SERVICE MODES , BUS MEAS [ON] , DC BUS . Then the abbreviated faulty power supply is displayed on the CRT. If the faulty power supply is +65 V, see the note below.
b. Continue with the *TROUBLESHOOT A2 POST-REGULATOR* in this chapter. In particular, check the faulty power supply.

Note

If the internal test 4 indicates +65 V power supply failure, there is a probability of the test failure caused by the A5 synthesizer or A6 receiver IF trouble. If the A2 post-regulator is verified in the *TROUBLESHOOT A2 POST-REGULATOR* , suspect the A5 synthesizer or the A6 receiver IF.

Note

The internal test 4: A2 POST REGULATOR is a built-in diagnostics test. The test checks all A2 power supply voltages within the limits using the DC BUS and the A/D converter on the A6 receiver IF. If a power supply failure is found, the HP 4286A stops the test process and displays the test result as shown in Figure 5-5. For more information about the internal test and the DC BUS, see Chapter 10.

FIND OUT WHY THE FAN IS NOT ROTATING

If the fan is not rotating, the problem may be in the A40 pre-regulator, the A2 post-regulator, or the fan.

1. Check the Line Voltage, Selector Switch Setting, and Fuse

Check the main power line cord, line fuse, line selector switch setting, and actual line voltage to see that they are all correct. Figure 5-6 shows how to remove the line fuse, using a small flat-bladed screwdriver to pry off the fuse holder. For more information about the line selector switch setting and the line cord, see the *Power Requirements* in Appendix C.

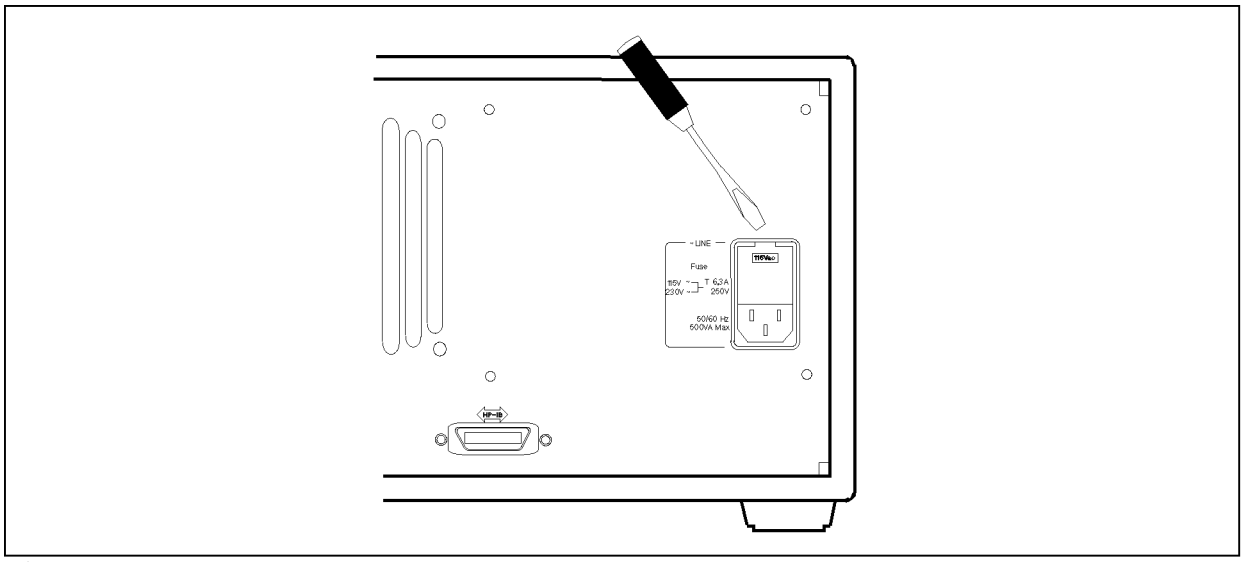

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Figure 5-6. Removing Line Fuse

2. Check the A40 SHUTDOWN LED

When the fan stops, the A40 SHUTDOWN LED lights. See the Figure 5-13 Power Supply Block Diagram 1. The fan generates a FAN LOCK signal. The signal is fed into the FAN LOCK SENSE circuit in the A40 pre-regulator. If the FAN stops, the FAN LOCK signal is missing. Then the FAN LOCK SENSE circuit activates the A40 shutdown circuitry, resulting the SHUTDOWN LED turned on.

Perform the following procedure to check the A40 SHUTDOWN LED on.

a. Remove the HP 4286A's top cover and shield plate.

b. Make sure the A2 post-regulator is firmly seated and the cable between A40J2 and A2J4 is connected properly.

c. Turn the HP 4286A power on.

d. Look at the A40 SHUTDOWN LED. The LED location is shown in Figure 5-2.

- If the SHUTDOWN LED is off, replace the A40 pre-regulator.
- If the SHUTDOWN LED is on, check the cable connection between A40J2 and A2J4. If the connection is good, continue with the *TROUBLESHOOT THE FAN AND THE A40 POST-REGULATOR* in this chapter.

FIND OUT WHY THE A40 SHUTDOWN LED IS ON

Use this procedure when the fan is rotating. If the fan is not rotating, see the *FIND OUT WHY THE FAN IS NOT ROTATING*.

If the fan is rotating, the A40 SHUTDOWN LED turning on indicates the A40 shutdown circuit is protecting the +5 VD power supply from the over voltage condition. The +5 VD power line may be shorted with one of power lines higher than +5 V. The problem may be in the A40 pre-regulator, the A2 post-regulator, and any of assemblies obtaining the power from +5 VD supply and the higher power supplies.

1. Disconnect the Cable from the A40J1

Turn the HP 4286A power off. Disconnect the cable from the A40J1. Turn the HP 4286A power on.

- If the A40 SHUTDOWN LED is still on, replace the A40 pre-regulator.
- If the A40 SHUTDOWN LED goes out, the A40 pre-regulator is verified. Turn the HP 4286A power off and reconnect the cable to the A40J1. Continue with the next *Disconnect the Cable from the A51J2*.

2. Disconnect the Cable from the A51J2

Turn the HP 4286A power off. Disconnect the cable from the A51J2. Turn the HP 4286A power on.

- If the A40 SHUTDOWN LED goes out, replace the A51 GSP.
- If the A40 SHUTDOWN LED is still on, the A51 GSP is verified. Turn the HP 4286A power off and reconnect the cable to the A51J2. Continue with the next *Disconnect the Cable from the A1J10*.

3. Disconnect the Cable from the A1J10

Turn the HP 4286A power off. Disconnect the cable from A1J10. Turn the HP 4286A power on.

- If the A40 SHUTDOWN LED goes out, replace the A1 CPU.
- If the A40 SHUTDOWN LED is still on, the A1 CPU is verified. Turn the HP 4286A power off and reconnect the cable to the A1J10. Continue with the next *Remove Assemblies*.

4. Remove Assemblies

a. Turn the HP 4286A power off.

b. Remove the assemblies, A3, A4, A5, and A6. Don't remove the A2 post-regulator.

c. Turn the HP 4286A power on.

- If the A40 SHUTDOWN LED is still on, the A2 post-regulator is probably faulty. Replace the A2 post-regulator. If the SHUTDOWN LED is still on after replacing the A2 post-regulator, inspect the A20 motherboard for soldering bridges and shorted traces on the FAN POWER and the FAN LOCK signal paths.
- If the A40 SHUTDOWN LED goes out, the A2 post-regulator and the A20 motherboard are verified. Continue with the next step.

d. Reinstall each assembly one at a time. Turn the HP 4286A power on after each is installed. The assembly that causes the A40 SHUTDOWN LED to go on is the most probable faulty assembly. Replace the assembly.

FIND OUT WHY THE A1 +5 VD LED IS NOT ON STEADILY

If the +5 VD LED is not on steadily, the +5 VD line voltage is missing or is not enough to power the HP 4286A. The problem may be in the A40 pre-regulator, the A1 CPU, and any of assemblies obtaining the power from +5 VD supply.

1. Check the A40 Pre-Regulator

a. Turn the HP 4286A power off.

b. Disconnect a cable form the A40J1. The A40J1 location is shown in Figure 5-7.

c. Turn the HP 4286A power on.

d. Check the voltage between the A40J1 pin 1 and pin 6 within +4.59 V to +5.61 V using a voltmeter with a small probe.

- If the voltmeter reading is out of the limits, replace the A40 pre-regulator.
- If the voltmeter reading is within the limits, the A40 +5 VD power supply is verified. Turn the HP 4286A power off and reconnect the cable to the A40J1. Then continue with the next *Disconnect Cables on the A1 CPU* section.

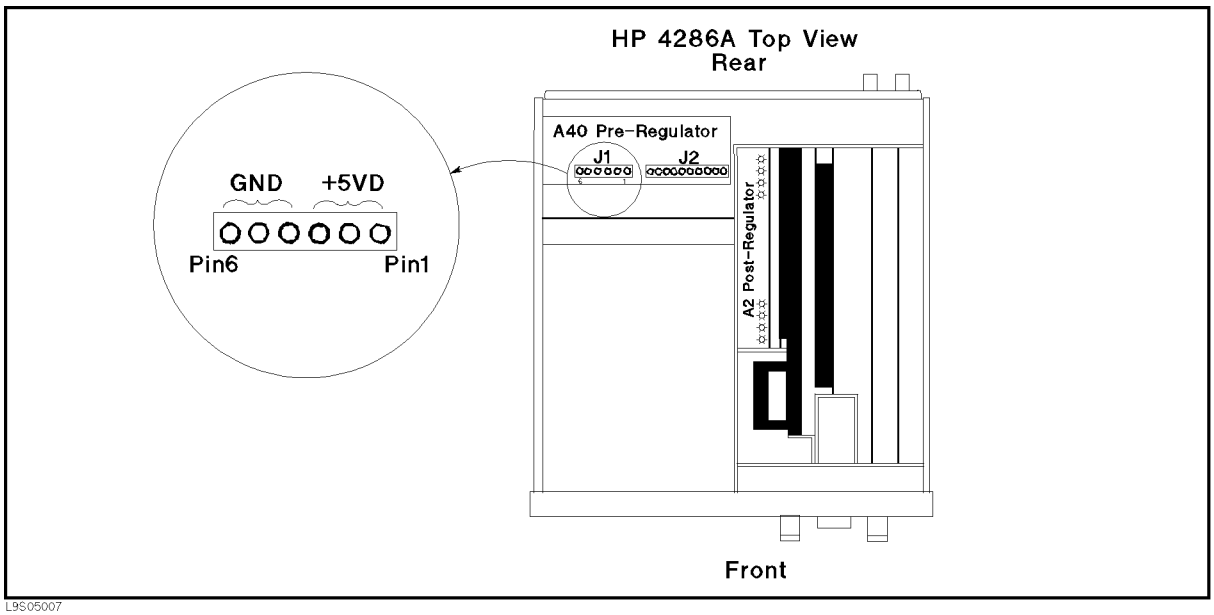

Figure 5-7. A40J1 Output Voltage

2. Disconnect Cables on the A1 CPU

a. Turn the HP 4286A power off.

b. Disconnect cables from the A1 CPU's connectors, J10, J11 (if option 1C2 installed), J12, J13, J14, J16, and J17. The connector locations are shown in Figure 5-8.

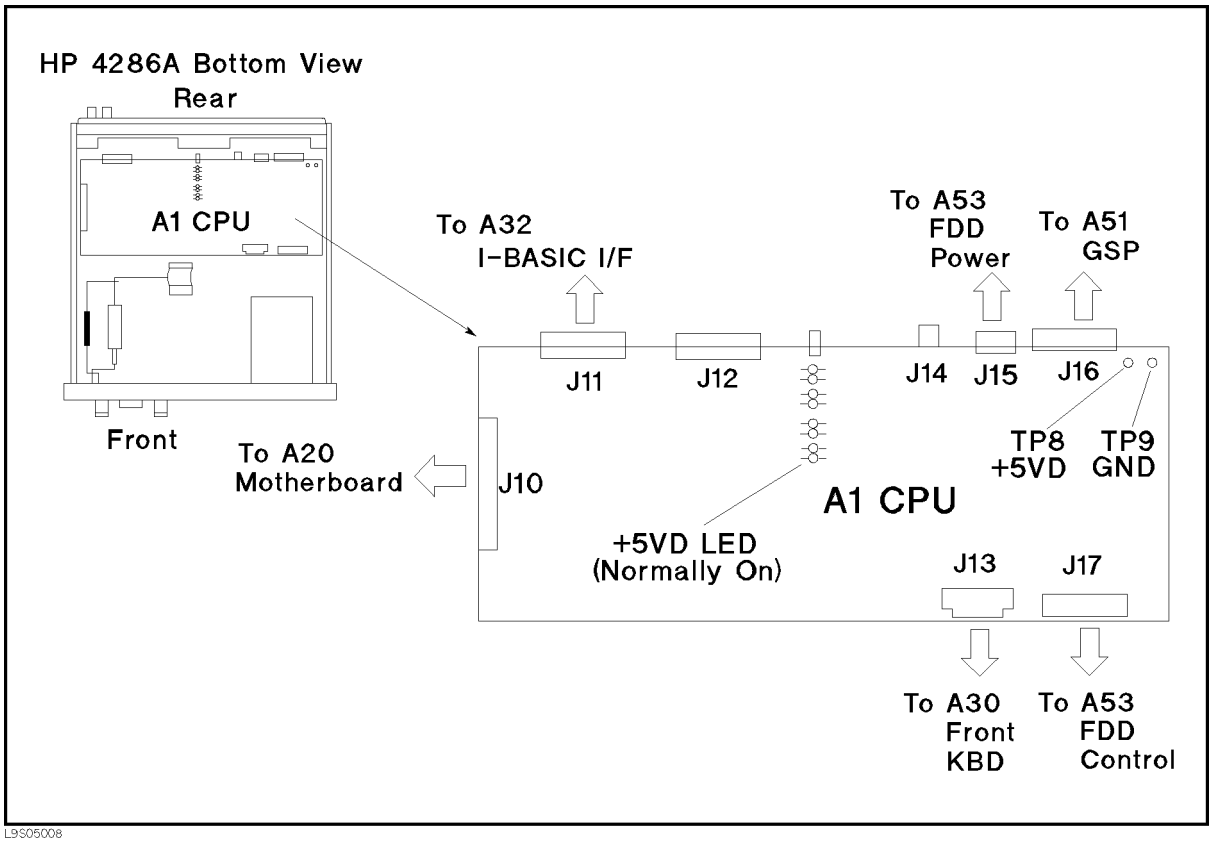

Figure 5-8. A1 CPU Connector Locations

c. Turn the HP 4286A power on. Look at the A1 +5 VD LED.

- If the LED is still off, the A1 CPU is probably faulty. Replace the A1 CPU.
- If the LED goes on, the A1 CPU is verified. Continue with the next step.

d. Turn the HP 4286A power off. Reconnect the cable to the A1J10. Turn the HP 4286A power on. Look at the A1 +5 VD LED.

- If the +5 VD LED goes out, the problem may be in the analog assemblies or the A33 handler interface. Continue with the next *Remove Assemblies*.
- If the + 5 VD LED is still on, continue with the next step.

e. Reconnect one of the disconnected cables to its connector at a time. Turn the HP 4286A power on after each cable is connected. The assembly related with the cable turning the +5 VD LED off is probably faulty. Replace the assembly.

3. Remove Assemblies

a. Turn the HP 4286A power off. Remove the assemblies, A3, A4, A5, A6, and A33. Do not remove the A2 post-regulator.

b. Turn the HP 4286A power on. Look at the A1 +5 VD LED.

- If the LED is still off, replace the A2 post-regulator. If the +5 VD LED is still off after replacing the A2 post-regulator, inspect the A20 motherboard for soldering bridges and shorted traces on the +5 VD power line.
- If the LED goes on, the A2 post-regulator and the A20 motherboard are verified. Continue with the next step.

c. Reinstall one of the removed assemblies at a time. Turn the HP 4286A power on after each is installed. The assembly that turns the A1 +5 VD LED on is the most probable faulty assembly. Replace the assembly.

TROUBLESHOOT THE FAN AND THE A40 PRE-REGULATOR

Perform the following procedure to troubleshoot the fan and the A40 pre-regulator.

1. Troubleshoot the Fan

a. Turn the HP 4286A power off.

b. Disassemble the rear panel in accordance with Chapter 13.

c. Remove the fan power cable from the A20J18.

d. Connect a DC power supply, a 10 kΩ resistance, and a oscilloscope to the fan power cable using appropriate wires as shown in Figure 5-9.

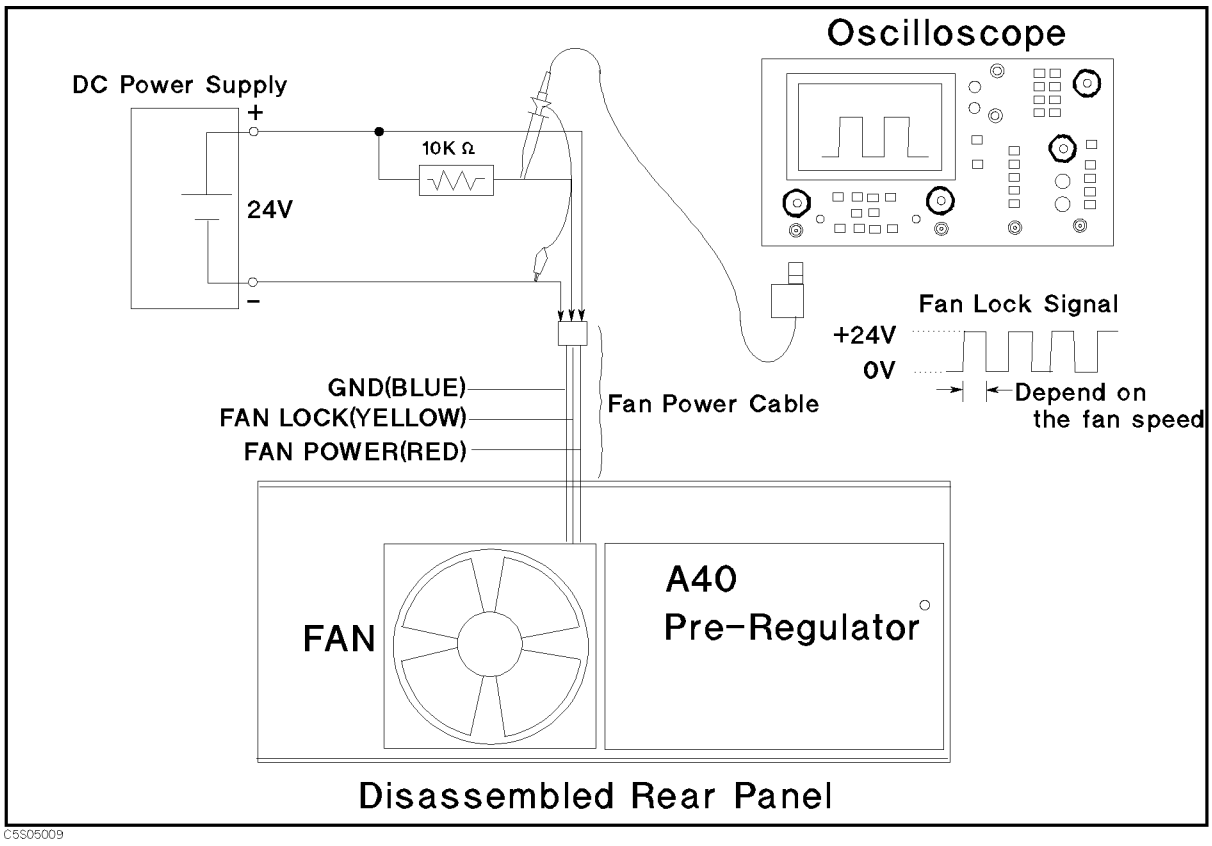

Figure 5-9. Fan Troubleshooting Setup

e. Turn the DC power supply on. Adjust the output voltage to +24 V.

f. Check the fan is rotating. Check the FAN LOCK signal is as shown in Figure 5-9.

- If the fan is not rotating or the FAN LOCK signal is unexpected, replace the fan.
- If these are good, the fan is verified. Continue with the next *Troubleshoot the A40 Pre-Regulator*.

2. Troubleshoot the A40 Pre-Regulator

a. Connect the fan power cable to the A40J2 using appropriate wires as shown in Figure 5-10.

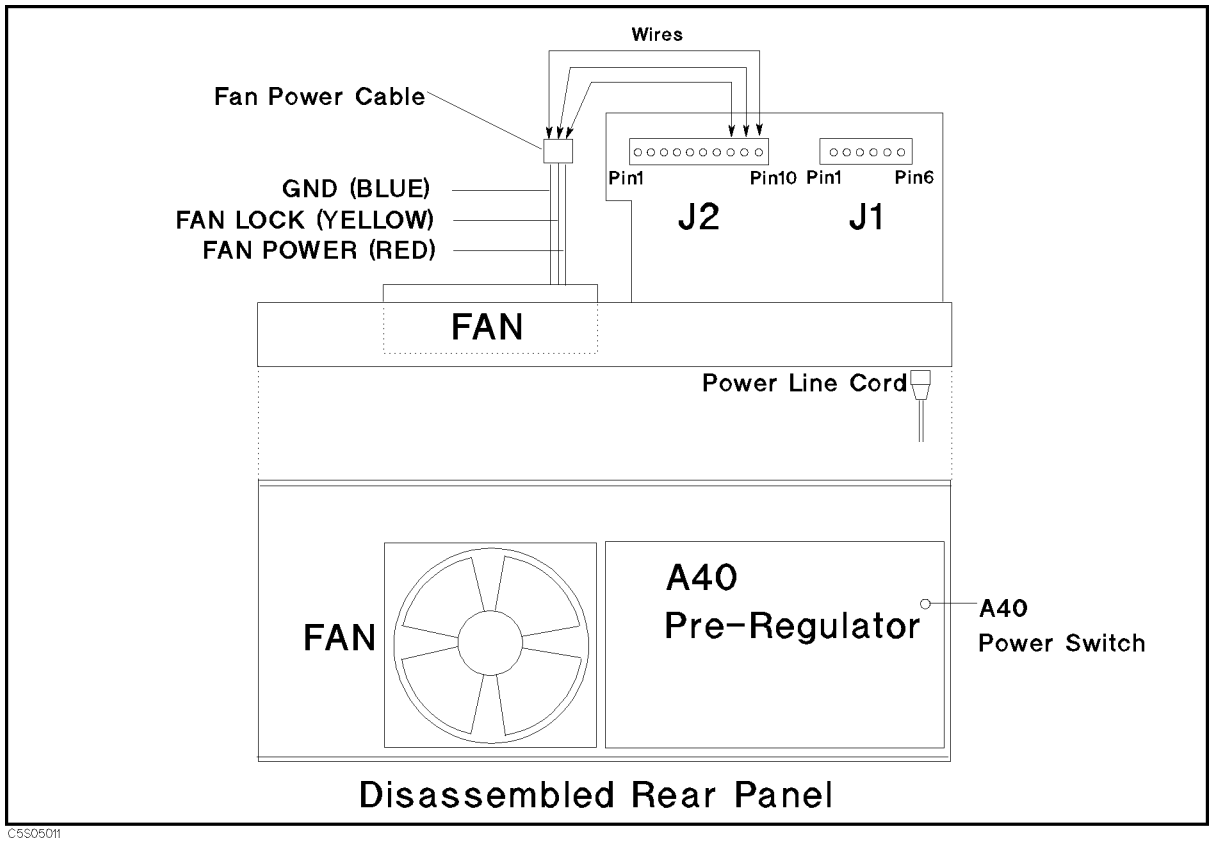

Figure 5-10. A40 Pre-Regulator Troubleshooting Setup

b. Connect the power cord to the A40 pre-regulator. Turn the A40 power on by pushing the A40 power switch. Then check the fan is rotating.

- If the fan is not rotating, check the connections between the fan power cable and the A40J2. If the connections are good, replace the A40 pre-regulator.
- If the fan is rotating, continue with the next step.

c. Measure all power supply voltages on A40J1 and A40J2 using a voltmeter with a small probe. See the Table 5-1 for power lines, connector pins, and limits.

Table 5-1. A40 Power Supplies

Supply	Connector Pin	GND Connector Pin	Range
+5 VD	A40J1 Pin 1, 2, and 3	A40J1 Pin 4, 5, and 6	+4.59 V to +5.61 V
-18 V	A40J2 Pin 1	A40J2 Pin 3 and 4	-14.4 V to -21.6 V
+18 V	A40J2 Pin 2	A40J2 Pin 3 and 4	14.4 V to 21.6 V
+7.8 V	A40J2 Pin 5	A40J2 Pin 3 and 4	6.24 V to 9.36 V
-7.8 V	A40J2 Pin 6	A40J2 Pin 3 and 4	-6.24 V to -9.36 V
+70 V	A40J2 Pin 7	A40J2 Pin 10	63 V to 77 V
+25 V	A40J2 Pin 8	A40J2 Pin 10	22.5 V to 27.5 V

- If any of the power supply voltages are out of the limits, replace the A40 pre-regulator.
- If all A40 power supply voltages are good, the A40 pre-regulator is verified. Reconnect the fan power cable to A20J18 and assemble the rear panel.

If the trouble still persists, inspect the fan power lines (FAN POWER, FAN LOCK) on the A2 post-regulator and A20 mother boards. Check the traces between the A2J4 and the A20J18 for soldering bridges and shorted traces.

TROUBLESHOOT THE A2 POST-REGULATOR

Use this procedure when the fan is rotating and the A40 SHUTDOWN LED turns off.

If one or some of the A2 eight LEDs are not on steadily, the corresponding A2 power supply voltages, -15 V, -5 V, +5 V, +5.3 V, +15 VD, +65 V, are missing or are not enough to power the HP 4286A. The problem may be in the A40 pre-regulator, the A2 post-regulator, and any of assemblies obtaining the A2 post-regulator.

1. Check the A40 Pre-Regulator

Turn the HP 4286A power on. Check the A40 power supply voltages within the limits using a voltmeter with a small probe. See the Table 5-2 for the power supplies, A2J4 pins, and the limits.

Table 5-2. A40 Power Supplies

Supply	Connector Pin	GND Connector Pin	Range
-18 V	A40J2 Pin 1	A40J2 Pin 3 and 4	-14.4 V to -21.6 V
+18 V	A40J2 Pin 2	A40J2 Pin 3 and 4	14.4 V to 21.6 V
+7.8 V	A40J2 Pin 5	A40J2 Pin 3 and 4	6.24 V to 9.36 V
-7.8 V	A40J2 Pin 6	A40J2 Pin 3 and 4	-6.24 V to -9.36 V
+70 V	A40J2 Pin 7	A40J2 Pin 10	63 V to 77 V
+25 V	A40J2 Pin 8	A40J2 Pin 10	22.5 V to 27.5 V

- If any of the line voltages are out of the limits, replace the A40 pre-regulator.
- If all voltmeter reading are within the limits, the A40 power supply is verified. Continue with the next *Remove Assemblies*.

2. Remove Assemblies

a. Turn the HP 4286A power off.

b. Remove the assemblies, A3, A4, A5, and A6. Don't remove the A2 post-regulator.

c. Turn the HP 4286A power on. Look at the A2 eight LEDs.

- If some LEDs are still off, replace the A2 post-regulator. If the trouble still persists after replacing the A2 post-regulator, inspect the A20 motherboard for soldering bridges and shorted traces.
- If all LEDs turns on, the A2 post-regulator and the A20 motherboard are verified. Continue with the next step.

d. Reinstall each assembly one at a time. Turn the HP 4286A power on after each is installed. The assembly that turns off some LEDs is the most probable faulty assembly. Replace the assembly.

3. Measure the A2 Post Regulator Output Voltages

Use this procedure to measure all A2 post-regulator voltages. If all A2 output voltages are within the limits, the A2 post-regulator is verified with 100% confidence.

This procedure put out the A2 post-regulator from the HP 4286A and measure the voltages on the A2J3 pins and A3J5 pins. A pulse generator is used to feed the substitute of the FAN LOCK signal to the A40 pre-regulator. This purposes not to shut down the A40 pre-regulator.

a. Turn the HP 4286A power off.

b. Remove the cable from A2J4.

c. Remove A2 post-regulator from the HP 4286A.

d. Reconnect the cable between the A2J4 and the A40J2 as shown in Figure 5-11.

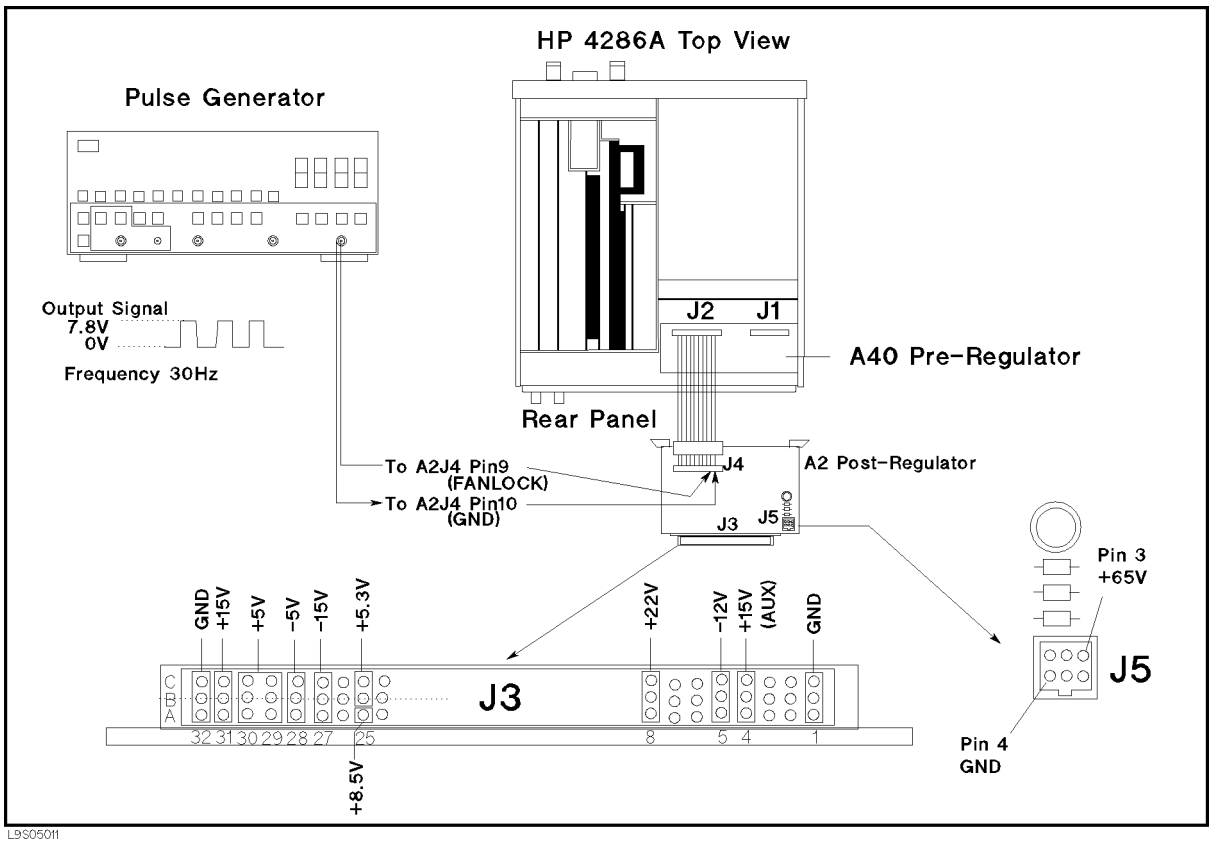

Figure 5-11. A2 Output Voltage Measurement Setup

e. Connect the pulse generator to the A2J4 as shown in Figure 5-11.

f. Turn the pulse generator power on. Set the controls as follows:

Wave Form	Square
Frequency	Approximately 30 Hz
Amplitude	+7.8 V

g. Turn the HP 4286A power on.

h. Measure the A2 output voltages at the A2J3 pins and A2J5 pins using a voltmeter with a small probe. See Figure 5-11 and Table 5-3 for the power supplies, A2J3 and A2J5 pins, and the limits.

Table 5-3. Power Supplies on A2 Post-Regulator

Supply	Connector Pin	Range
+22 V	J3 Pin 8	19.8 V to 24.2 V
+15 V(AUX)	J3 Pin 4	13.5 V to 16.5 V
+15 V	J3 Pin 31	13.5 V to 16.5 V
+8.5 V	J3 Pin 25C	7.65 V to 9.35 V
+5.3 V	J3 Pin 25A 25B	4.77 V to 5.83 V
+5 V	J3 Pin 30 29	4.5 V to 5.5 V
-5 V	J3 Pin 28	-4.5 V to -5.5 V
-12 V	J3 Pin 5	-10.8 V to -13.2 V
-15 V	J3 Pin 27	-13.5 V to -16.5 V
FAN POWER	J3 Pin 8	19.2 V to 28.8 V
+65 V	J5 Pin 3	58.5 V to 71.5 V
GND	J3 Pin 3,4,10	
	J5 Pin 4	

- If any of the line voltages are out of the limits, replace the A2 post-regulator.
- If all line voltages are within the limits, the A2 post-regulator is verified.

TROUBLESHOOT THE A52 DC-DC CONVERTER

The A52 DC-DC converter obtains the +65 V voltage from the A2 post-regulator, and supplies the +15.75 V voltage to the A51 GSP and the CRT display.

To check the A52 output voltage, disconnect the flat cables from A52J1 (the cable to the CRT display) and A52J3 (the cable to the A51 GSP). Then measure the voltage at A52TP4. When the flat cables of A52J1 and A52J3 are disconnected, the A52TP4 voltage is typically +16.5 V ± 1 V.

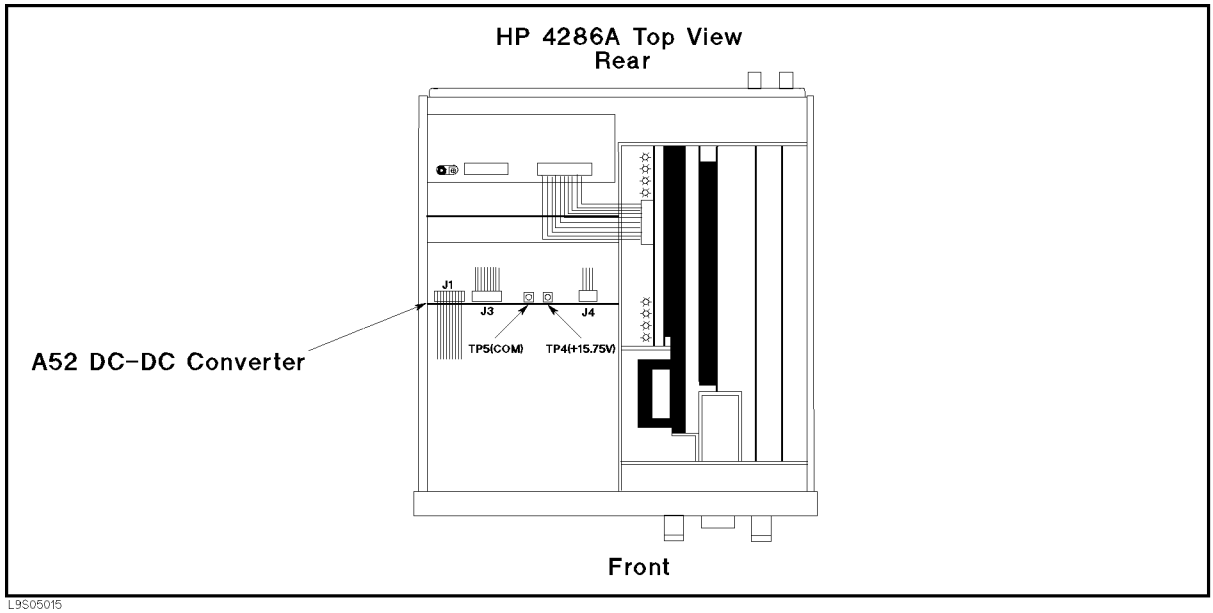

Figure 5-12. A52 Test Point

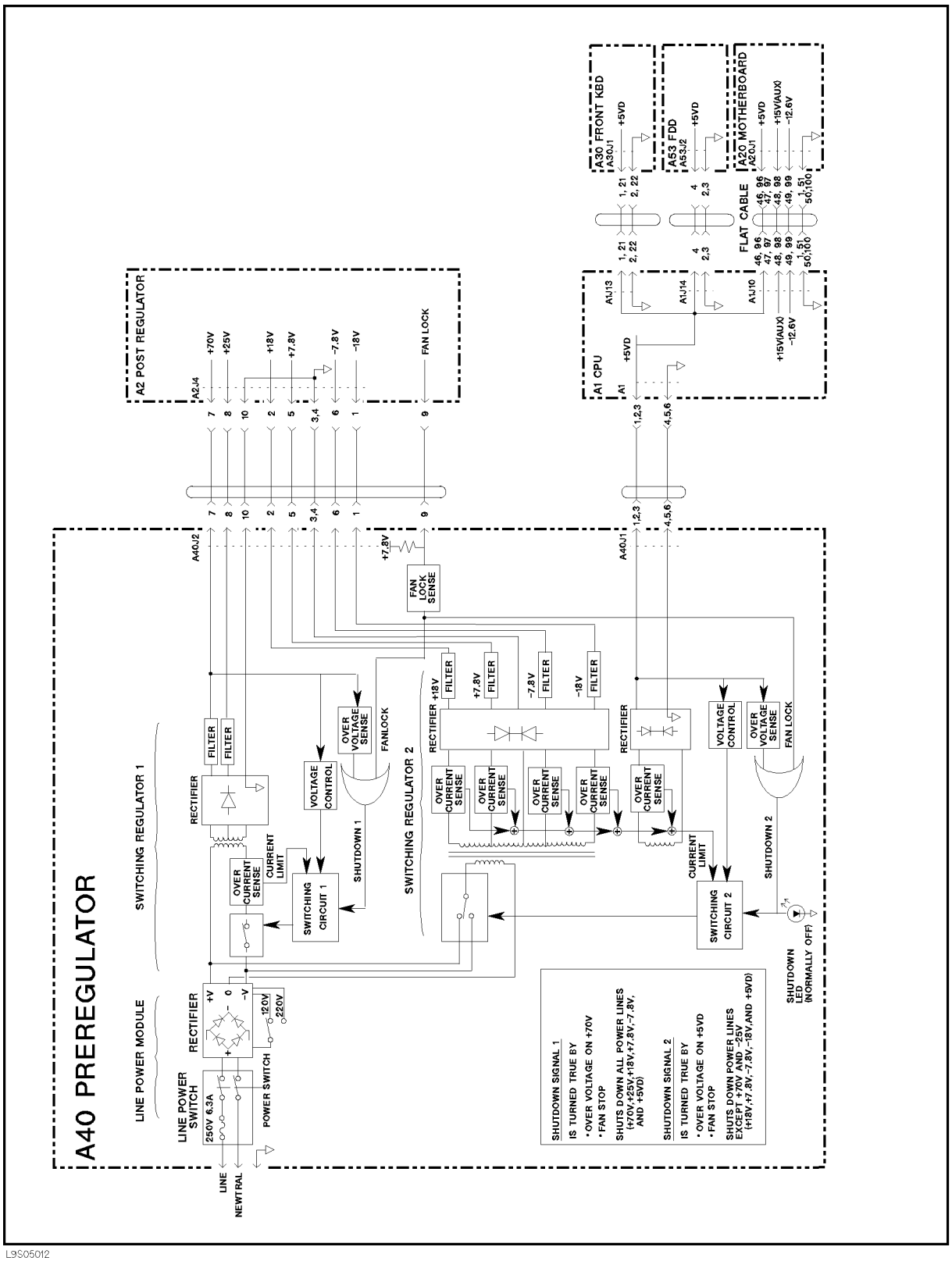

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Figure 5-13. Power Supply Block Diagram 1

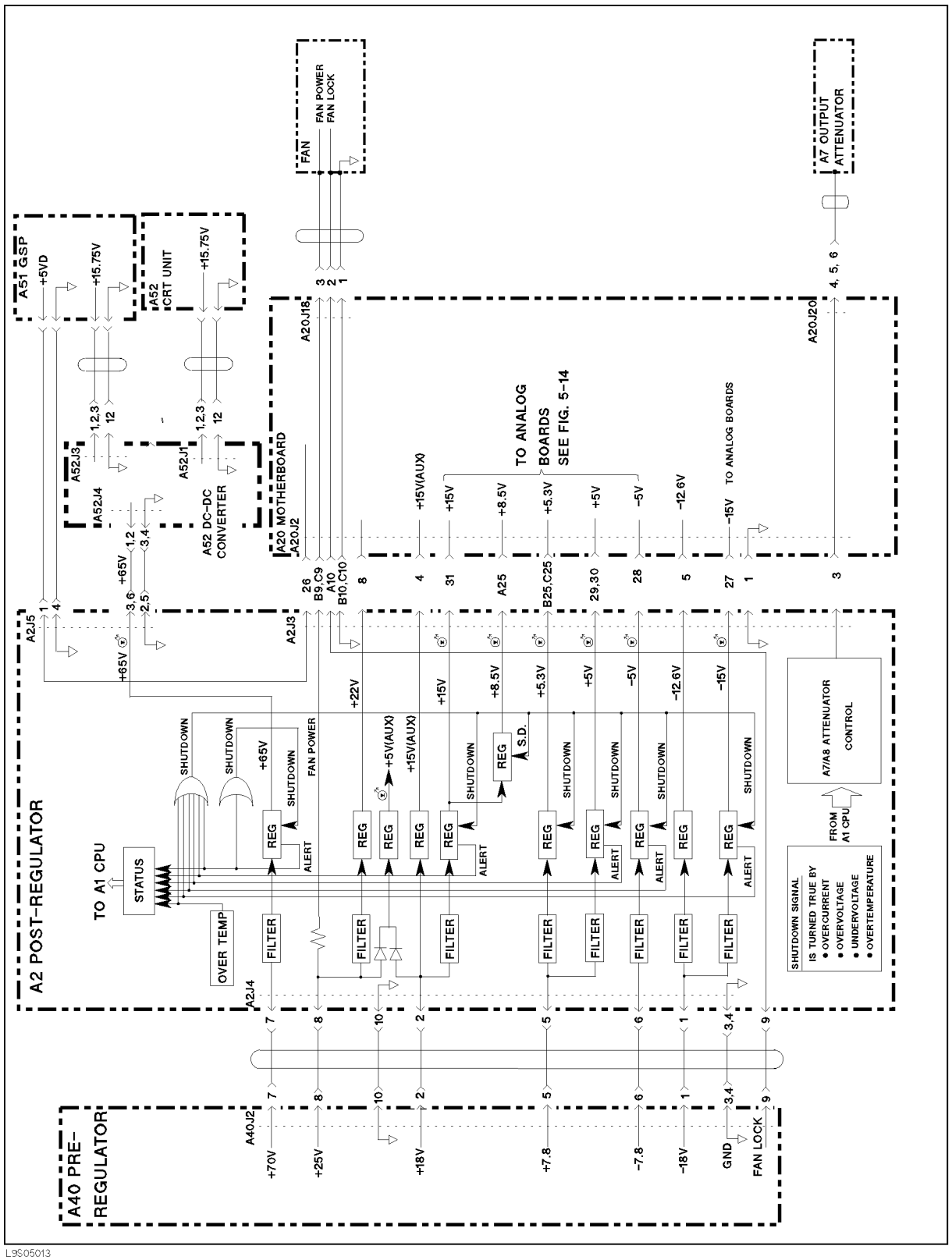

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Figure 5-14. Power Supply Block Diagram 2

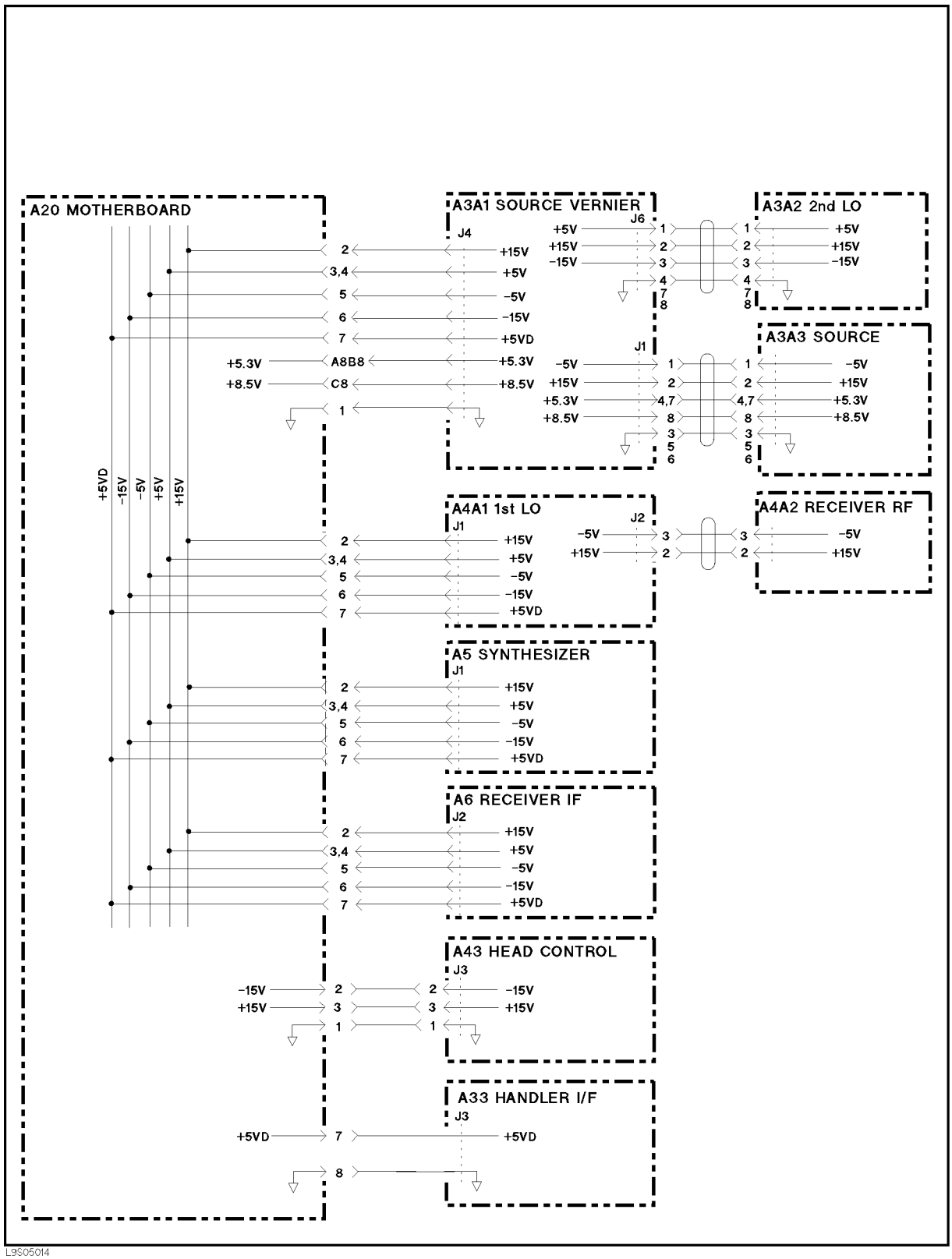

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Figure 5-15. Power Supply Block Diagram 3

6

Digital Control Troubleshooting

INTRODUCTION

Use this procedure only if you have followed the procedures in Chapter 4, and believe the problem to be in the digital control group. This procedure is designed to let you identify the bad assembly within the digital control group in the shortest possible time. Whenever an assembly is replaced in this procedure, see the *Table of Related Service Procedures* in Chapter 14.

Figure 6-1 shows the digital control group in simplified block diagram form. The following assemblies make up the digital control group:

- A1 CPU
- A31 Interface Connector
- A30 Front Keyboard
- A32 I-BASIC Interface
- A51 GSP
- CRT display
- Flexible Disk Drive

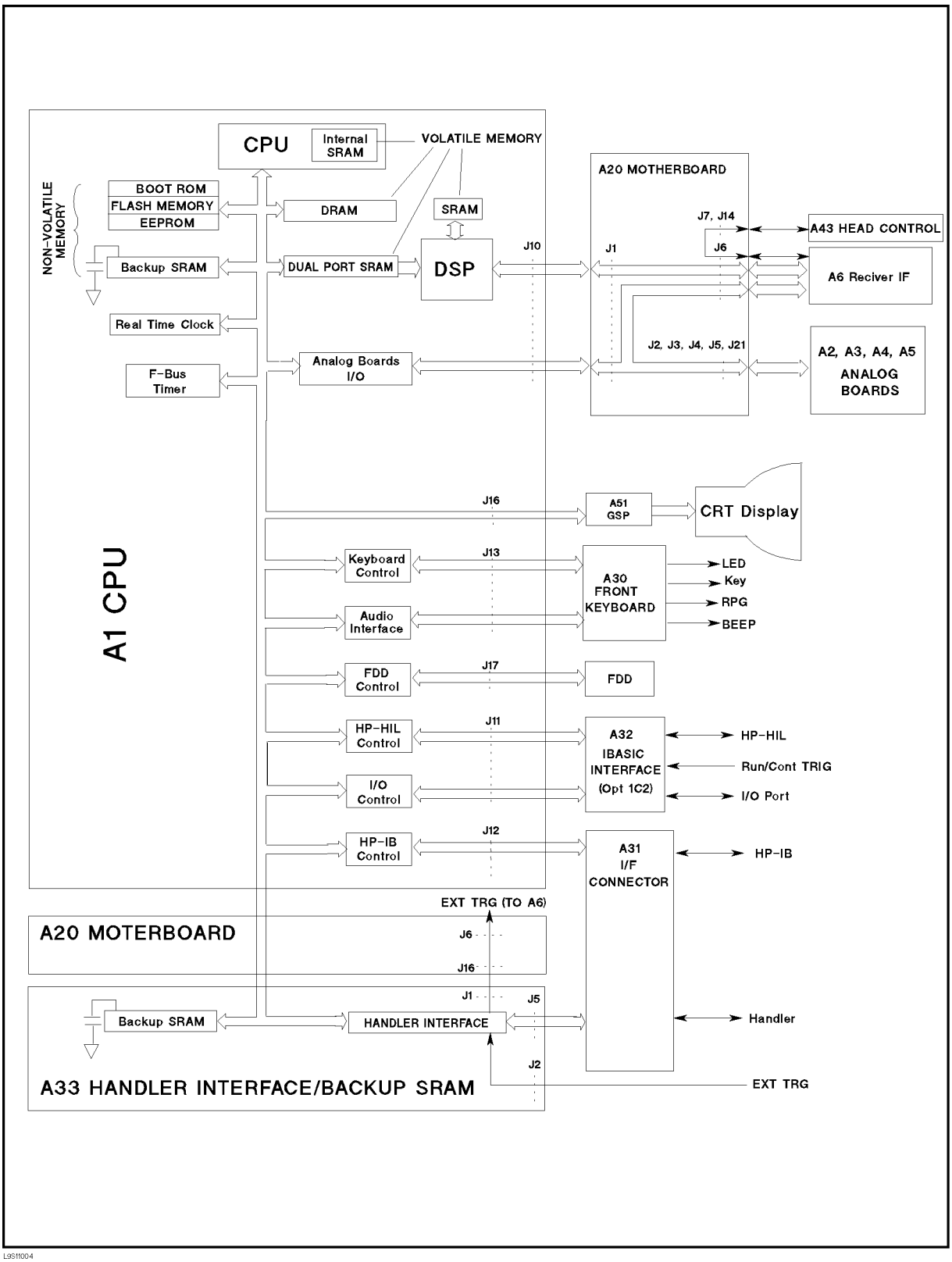

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Figure 6-1. Digital Control Group Simplified Block Diagram

DIGITAL CONTROL TROUBLESHOOTING SUMMARY

This summary gives an overview of the digital control group troubleshooting procedure. Technicians who are already familiar with troubleshooting the digital control group may save time by following this summary instead of reading the entire procedure. Headings in this summary match the headings in the procedure.

Start Here

1. Check the Power On Sequence.
   Check the eight A1 LEDs.
2. Check Error Messages.
   Identify the First Failed Test.
3. Check the A1 DRAM and Flash Memory.
   Access the bootloader menu. Then check error messages.
4. Check the A1 Volatile Memory.
   Run external test 2.
5. Check the A30 Front Keyboard.
   Run external test 16.
6. Check the A33 Handler Interface / Backup SRAM.
   Run internal test 15.
   Run external test 25.
7. Check the Flexible Disk Drive.
   Run external test 17.
8. Check the A32 I-BASIC Interface and the HP-HIL Keyboard (Option 1C2).

Troubleshoot the A51 GSP

1. Run the Internal Test 3: A51 GSP.
2. Check the two LEDs on the A51 GSP.

START HERE

1. Check the Power On Sequence

Turn on the HP 4286A and watch for the following events in this order:

a. Beep is sounds in approximately 1 second.
b. CRT display comes up bright and focused.

- If the power on sequence is good, continue with *2. Check Error Messages* in this section.
- In case of unexpected results, continue with the next step.

Check the Eight A1 LEDs

There are eight LEDs on the A1 CPU. At the end of the power on sequence, these LEDs should be in pattern 1 as shown in Figure 6-2. Perform the following procedure to check the eight A1 LEDs.

a. Turn the HP 4286A off.

b. Remove the bottom cover of the HP 4286A.

c. Turn the HP 4286A power on.

d. Look at the eight A1 LEDs. Some of the LEDs light during the power on sequence. At the end of the power on sequence, the LEDs should stay in pattern 1 shown in Figure 6-2.

   - If the LEDs stay in pattern 1, the A1 CPU is probably working.
   - If the LEDs stay in any of the fixed patterns 2 through 8 shown in Figure 6-2, the trouble is in the power supply functional group. Continue with Chapter 5.
   - If the LEDs stay in any pattern other than patterns 1 through 8, the A1 CPU is probably faulty. Replace the A1 CPU.

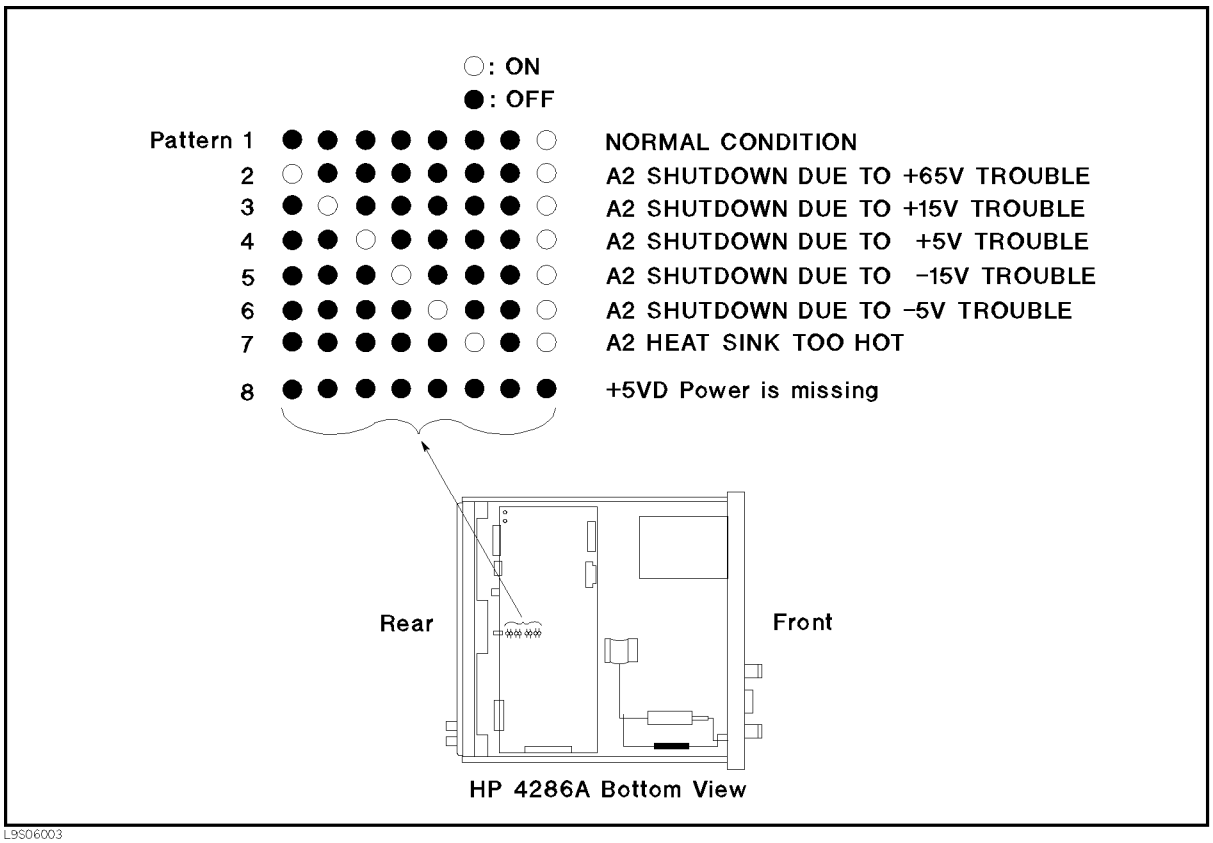

Figure 6-2. Eight A1 LEDs Patterns

2. Check Error Messages

Turn the HP 4286A power on. Check that no error message appears on the CRT.

- If no error message is displayed, continue with *3. Check the A1 DRAM and Flash Memory* .
- If one of error messages listed below is displayed, follow the associated instruction. For any other message, see *Error Messages* in Messages.

Error Messages	Instruction
`POWER ON TEST FAILED`	This indicates the power on self-test failed. Continue with the next *Identify First Failed Test*
`EEPROM CHECK SUM ERROR`	This indicates that the correction constants stored in the EEPROM on the A1 CPU are invalid or the EEPROM is faulty. Rewrite all correction constants into the EEPROM using the adjustment program (PN 04286-65002). For the detailed procedure, see Chapter 3. If the rewriting is not successfully performed, replace the EEPROM. Then rewrite all correction constants into the new EEPROM.
`Svc` (Status Annotation)	This indicates that the correction constants stored in the EEPROM on the A1 CPU are invalid or the EEPROM is faulty. See the instruction for the `EEPROM CHECK SUM ERROR` message above.

Identify the First Failed Test

If the power on self-test fails and the "POWER ON TEST FAILED" message is displayed, execute the ALL INT test to identify the first failed test, using the following procedure. If internal test 1: A1CPU is the first failed test, replace the A1 CPU. Otherwise see Chapter 4.

a. Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (0), and (x1) to access internal test 0: ALL INT.

b. Press EXECUTE TEST to execute the ALL INT test.

c. Wait until the test result (PASS or FAIL) is displayed.

d. Press the (⇧), (⇩) keys to find the first occurrence of a FAIL message for test 1 and tests 4 through 14.

3. Check the A1 DRAM and Flash Memory

The A1 DRAM and flash memory are tested on the sequence to access the bootloader menu. For the bootloader menu, see Chapter 10.

Perform the following procedure to verify the A1 DRAM and flash memory:

a. Turn the HP 4286A power off.

b. Press both the (Start) and (Preset) keys. With pressing both keys, turn the HP 4286A power on.

c. Wait until the display shown in Figure 6-3 appears on the CRT display.

d. Check that no error message is displayed on the CRT.

- If no error message is displayed, the A1 DRAM and flash memories are verified. Continue with *4. Check the A1 Volatile Memory* .
- If an error message is displayed or the display shown in Figure 6-3 does not appear, the A1 CPU is probably faulty. Replace the A1 CPU.

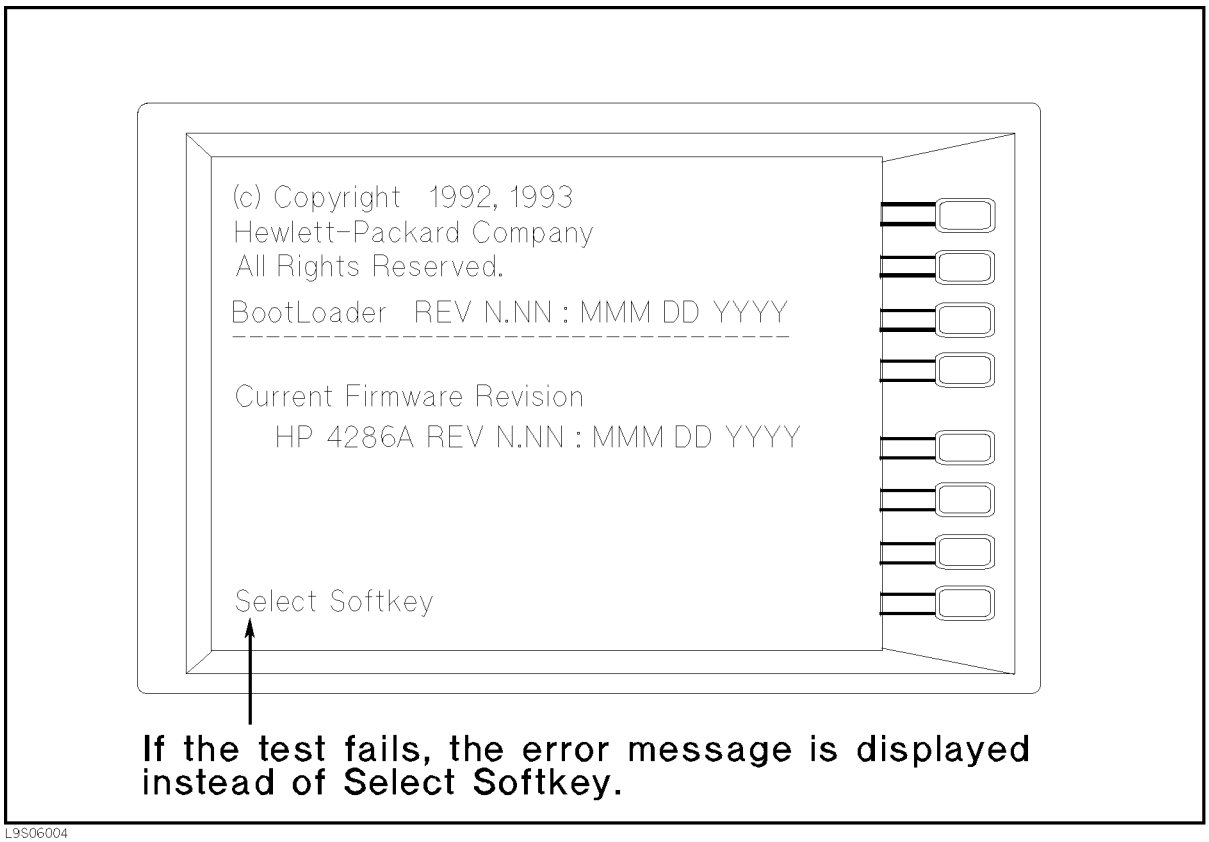

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Figure 6-3. Bootloader Display

4. Check the A1 Volatile Memory

a. Turn the HP 4286A power on.

b. Press (System), SERVICE MENU, TESTS, (2), (x1), EXECUTE TEST to run internal test 2: A1 VOLATILE MEMORY.

c. Check that no error message is displayed. At the end of this test, the HP 4286A returns the control settings to the default values (power on reset). If the test fails, the HP 4286A displays an error messages for a few seconds before returning to the defaults.

- If no error message is displayed, the A1 volatile memories are verified. Continue with *5. Check the A30 Front Keyboard.*
- If one of the error messages listed below is displayed, the A1 CPU is faulty. Replace the A1 CPU.

```
CPU INTERNAL SRAM R/W ERROR
DSP SRAM R/W ERROR
DUAL PORT SRAM R/W ERROR
CPU BACKUP SRAM R/W ERROR
```

5. Check the A30 Front Keyboard

The A30 front keyboard can be checked using external test 16: FRONT PANEL DIAG.

a. Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (1), (6), (x1), EXECUTE TEST to run external test 16.

b. Press all of the front panel keys. The abbreviated key name should be displayed when a key is pressed. Therefore, you can check every key on the A30 Keyboard except for (PRESET). (If you want to exit this test, press (PRESET).)

- If one or more keys seems to be defective, replace the A30 front keyboard.
- If all keys are good, the A30 front keyboard is verified. Continue with *6. Check the A33 Handler Interface / Backup SRAM.*

6. Check the A33 Handler Interface / Backup SRAM

Check the Backup SRAM

a. Press (Preset), (System), SERVICE MENU, TESTS, (1), (5), (x1), EXECUTE TEST, CONT to run internal test 15. The test takes about one minute.

b. After the HP 4286A is set to the power on state, press (System), SERVICE MENU, TESTS, (1), (5), (x1) and check the test result.

- If this test passes, continue with the next step.
- If this test fails, replace the A33 handler interface / backup SRAM.

Check the Handler Interface Function

a. Turn the HP 4286A off and remove the HP 4286A top cover.

b. Set the toggle switch and bit switches of the A33 board to the factory default setting shown on the HP 4286A top shield cover.

c. Connect the handler simulator (PN 04278-65001) to the HP 4286A rear panel handler interface connector.

d. Turn the HP 4286A on.

e. Press (Preset), (System), SERVICE MENU, TESTS, (2), (5), (x1), EXECUTE TEST to run external test 25.

f. If all the LEDs (except the LEDs that are not used. See Table 6-1.) on the handler simulator simultaneously blink several times, the handler interface function is good.

- If the result is good, continue with *Check the Flexible Disk Drive.*
- If the result is bad, check the flat cable to the A31 interface connector and the A31 interface connector. If no trouble is found, replace the A33 handler interface / backup SRAM.

Table 6-1. Handler Interface Function Test

Handler Simulator LED No.	HP 4286A Signal To Be Tested
LED1 (BIN1) to LED9 (BIN9)	/BIN1 to /BIN9
LED10 (OUT OF BIN)	/OUT OF BIN
LED11 (BIN10)	/AUX BIN
LED12 (PHI)	/PHI
LED13 (PLO)	/PLO
LED14 (SREJ)	/SREJ
LED15 (OVFL)	/FAIL
LED16 (UNDFL)	(Not used)
LED17 (UNBAL)	/NO CONTACT
LED18 (EOM)	/EOM
LED19 (EXT TRG)	(Not used)[1]
LED20 (INDEX)	/INDEX
LED21 (ALARM)	/ALARM
LED22 (CH1) to LED25 (CH.4)	(Not used)[1]

1 Ignore these LEDs.

7. Check the Flexible Disk Drive

The FDD (Flexible Disk Drive) can be checked using external test 17: DISK DR FAULT ISOL'N.

a. Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (1), (7), (x1), EXECUTE TEST to run external test 17.

b. As the HP 4286A instructs, insert a flexible disk into the FDD. Use a formatted but blank flexible disk. Otherwise, the data on the disk will be overwritten by this test. Then press CONT.

c. Check the test result (PASS or FAIL) that is displayed at the end of the test.

- If this test fails, replace the FDD.

8. Check the A32 I-BASIC Interface and the HP-HIL Keyboard (Option 1C2)

When Option 1C2 (I-BASIC) is installed, perform this procedure to verify the A32 I-BASIC interface assembly on the rear panel (Option 1C2 only). The HP-HIL external keyboard is connected to the A32 I-BASIC I/O connector, and is used to develop programs.

If the HP HIL keyboard of I-BASIC is not working, perform the following procedure to verify the HP HIL keyboard.

Press (PRESET), (SYSTEM), SERVICE MENU, TESTS, (1), (x1), EXECUTE TEST to run internal test 1: A1 CPU.

- If internal test 1 passes, the HP HIL driver circuit on the A1 CPU is probably working. Inspect cables between the HP HIL keyboard and the A1 CPU through the A32 I-BASIC interface. If the cable is good, replace the HP-HIL keyboard.
- If internal test 1 fails, replace the A1 CPU.

TROUBLESHOOT THE A51 GSP

1. Run Internal Test 3: A51 GSP

The A51 GSP can be checked using the internal test 3: A51 GSP.

a. Press (Preset), (System), SERVICE MENU, TESTS, 3, (x1) EXECUTE TEST to run the internal test 3.

b. After the HP 4286A is set to the power-on state, press (System), SERVICE MENU, TESTS, 3, (x1) to check the test result.

- If the test passes, continue with the next step.
- If the test fails, replace the A51 GSP.

2. Check Two LEDs on A51 GSP

There are two LEDs (A51DS1: BLANKING and A51DS2: +15.3 V) on the A51 GSP. They are normally on when the HP 4286A power is on.

- If the A51DS2 LED is off, +15.3 V for the CRT display is not being supplied by the A40 pre-regulator. See Chapter 5.
- If the A51DS1 LED is off, the A51 GSP synchronized clocks are not working properly. Replace the A51 GSP.

7

Source Group Troubleshooting

INTRODUCTION

Use these procedures only if you have read Chapter 4 and you believe the problemis in the source group.

This procedure is designed to let you identify the bad assembly within the source group in the shortest possible time. Whenever an assembly is replaced in this procedure, refer to Chapter 14.

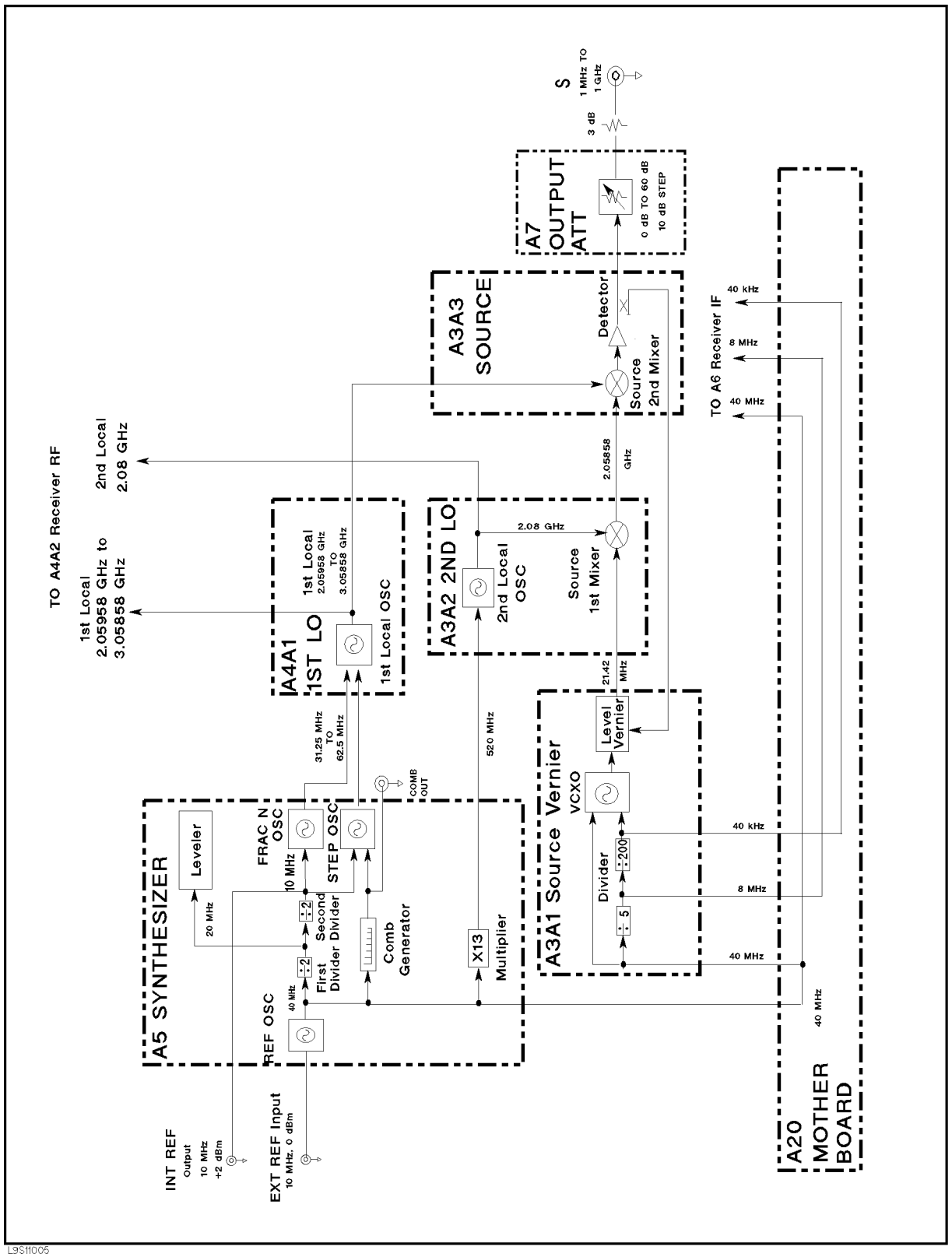
Figure 7-1 shows a simplified block diagram of the source group. The source group consists of the following assemblies:

- A5 Synthesizer
- A4A1 1st LO
- A3A1 Source Vernier
- A3A2 2nd LO
- A3A3 Source
- A7 Output Attenuator

Note

Make sure all of the assemblies listed above are firmly seated before performing the procedures in this chapter.

Allow the HP 4286A to warm up for at least 30 minutes before you perform any procedure in this chapter.



L9S11005

Figure 7-1. Source Group Block Diagram

SOURCE GROUP TROUBLESHOOTING SUMMARY

This overview summarizes the sequence of checks included in this chapter. Experienced technicians may save time by following this summary instead of reading the entire procedure. Headings in this summary match the headings in the procedure.

Start Here

1. Run internal test 10. If the test fails, check the INT REF signal. If the INT REF signal is good, replace the A3A1 Source Vernier. If the INT REF signal is bad, replace the A5 Synthesizer.
2. Run internal test 5. If the test fails, replace the A6 Receiver IF in the receiver group.
3. Run internal test 6. If the test fails, replace A5.
4. Run internal test 7. If the test fails, replace A5.
5. Run internal test 8. If the test fails, replace the A4 1st LO/Receiver RF.
6. Run internal test 12. If the test fails, replace the A3A1 Source Vernier.
7. Run internal test 9. If this test fails, replace the A3A2 2nd LO.
8. Run external test 19. If this test fails, check the A7 Output Attenuator control signals in accordance with the *Check A7 Output Attenuator Control Signals* section in this chapter.

Check A5 Synthesizer Outputs

1. Check the INT REF signal. If it is bad, replace A5.
2. Check the FRAC N OSC signal. If it is bad, replace A5.
3. Check the 520 MHz signal. If it is bad, replace A5.
4. Check the EXT REF operation. If it is bad, replace A5.

Check A4A1 1st LO Outputs

1. Check the 1st local oscillator signal at A4A1J3. If it is bad, replace A4.
2. Check the 1st local oscillator signal at A4A1J4. If it is bad, replace A4.

Check an A3A1 Source Vernier Output

1. Check the 21.42 MHz signal. If it is bad, replace A3A1.

Check A3A2 2nd LO Outputs

1. Check the 2nd local oscillator signal. If it is bad, replace A3A2.
2. Check the 2.05858 GHz signal. If it is bad, replace A3A2.

Check A3A3 Source Output

1. Check the A3A3 RF signal. If it is bad, replace A3A3.

Check A7 Output Attenuator Control Signals

1. Check the A7 control signals. If the control signals are bad, replace A2.

START HERE

The following procedure verifies the operation of each assembly in the source group by using the HP 4286A's self-test functions (internal and external tests). For detailed information about the self-test functions, see the *Service Key Menus*.

In this procedure, the A3A1's divider and the A6's A/D converter (receiver group) are verified first. This is done because the internal tests use the A/D converter to measure voltages at DC bus nodes within the source group. Also, the A3A1's divider output is used to generate the A/D converter's control signals.

Perform the following steps to troubleshoot the source group:

1. Press (Preset), (System), SERVICE MENUS, TESTS, (1), (0), (x1), EXECUTE TEST to run internal test 10: A3A1 DIVIDER.
   - If the test fails, there is a possibility that the A5 synthesizer is faulty. This possibility exists because the A3A1 divider obtains the 40 MHz reference signal from A5. Perform the *1. Check the INT REF Signal* procedure in the *Check A5 Synthesizer Outputs* section. This procedure verifies the 40 MHz reference signal. If the INT REF signal is good, A3A1 is probably faulty. Replace A3A1. If the INT REF signal is bad, replace A5.
2. Press (5), (x1), EXECUTE TEST to run internal test 5: A6 A/D CONVERTER. If the test fails, replace A6.
3. Press (6), (x1), EXECUTE TEST to run internal test 6: A5 REFERENCE OSC. If the test fails, replace A5.
4. Press (7), (x1), EXECUTE TEST to run internal test 7: A5 FRACTIONAL N OSC. If the test fails, replace A5.
5. Press (8), (x1), EXECUTE TEST to run internal test 8: A4A1 1st LO OSC. If the test fails, replace A4.
6. Press (1), (2), (x1), EXECUTE TEST to run internal test 12: A3A1 SOURCE OSC. If the test fails, replace A3A1.
7. Press (9), (x1), EXECUTE TEST to run internal test 9: A3A2 2ND LO OSC. If the test fails, replace A3A2.
8. Press (1), (9), (x1), EXECUTE TEST to run external test 19: OUTPUT ATTENUATOR. Then connect the front S and R connectors, and press CONTINUE to start the test. If the test fails, the A7 Output Attenuator is probably faulty. Perform the procedure provided in the *A7 Output Attenuator Control Signals* section to confirm that A7 is faulty.

If all the tests listed above pass and you still believe that the problem is in the source group, verify all the outputs of each assembly in the source group. The procedures to do this are provided in the following sections.

CHECK A5 SYNTHESIZER OUTPUTS

The output signals from the A5 Synthesizer are listed below. The input signal to A5 is the external reference signal from the EXT REF connector. See Figure 7-1. If all the output signals and the HP 4286A operation using the EXT REF input signal are good, A5 is probably good.

- INT REF signal on the rear panel
- FRAC N OSC signal going to A4A1
- 520 MHz signal going to A3A2
- 40 MHz signal going to A3A1 and A6

Perform the following procedures sequentially to verify all the signals listed above and to verify the HP 4286A operation when the EXT REF signal is used.

In these procedures, the 40 MHz signal is not verified because it is indirectly verified if the INT REF signal is good. The signals are observed using test equipment and the HP 4286A self-test functions. For detailed information about the self-test functions, see the *Service Key Menus*.

1. Check the INT REF Signal

The INT REF signal (10 MHz, +2 dBm typical) on the rear panel is derived from the 40 MHz reference signal through the first and second 1/2 dividers. See the A5 Synthesizer block in Figure 7-1. Perform the following steps to verify the INT REF signal's frequency and level:

a. On the HP 4286A, press the following keys to measure the INT REF frequency by using the bus measurement function:

   (Preset), (System), SERVICE MENU, SERVICE MODES, BUS MEAS [OFF], FREQ BUS [OFF], (5), (x1), BUS MEAS on OFF (then the label changes to BUS MEAS ON off)

b. Check that the monitor value displayed in the "X: " field is 2.5 U ± 0.01 U.

   The frequency bus measures the INT REF frequency (10 MHz) through a 1/4 divider. Therefore, the measured value is 2.5 U (10 MHz divided by 4). The unit "U" in the frequency bus measurement is equivalent to MHz.

   - If the monitor value is good, continue with the next step.
   - If the monitor value is bad, the second 1/2 divider in A5 is probably faulty. Replace A5.

c. Connect the equipment as shown in Figure 7-2.

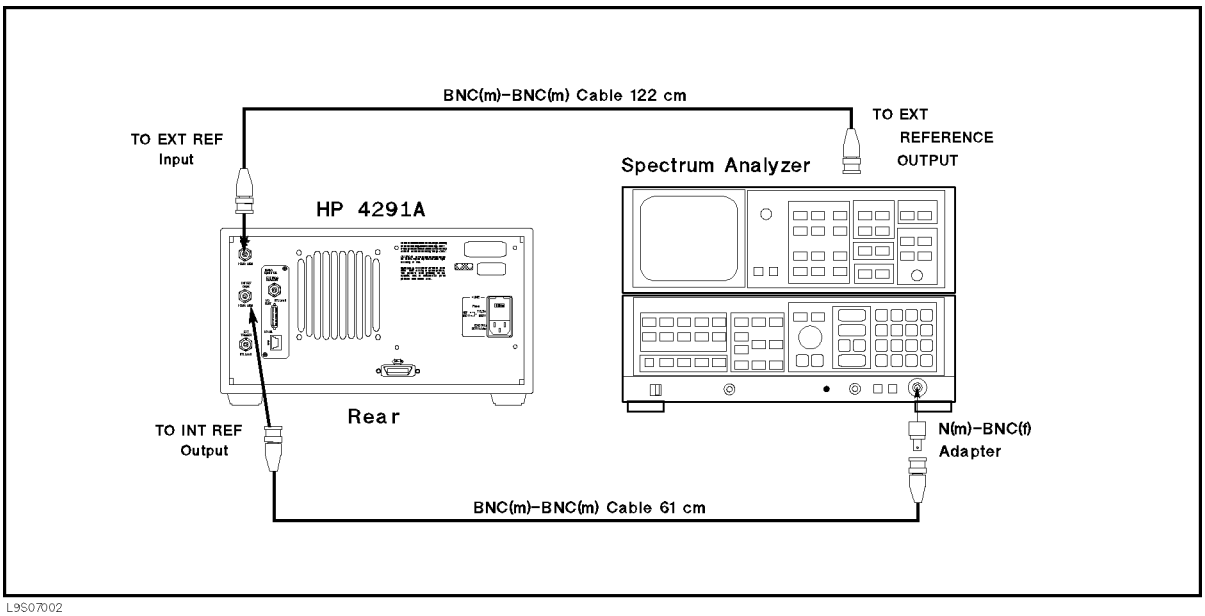


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Figure 7-2. INT REF Test Setup

d. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	**Settings**
Center Frequency	10 MHz
Span	15 MHz
Reference Level	10 dBm

e. On the spectrum analyzer, press (PEAK SEARCH) to move the marker to the peak of the INT REF signal.

f. Check that the frequency is approximately 10 MHz and the level is +2 dBm ± 4 dB. The INT REF signal should be as shown in Figure 7-3.

- If the INT REF signal is good, continue with *2. Check the FRAC N OSC Signal.*
- If the INT REF signal is bad, inspect the cable and connections between the INT REF connector and A5J10. See Figure 7-2 for the location of A5J10. If the cable and connections are good, replace A5.

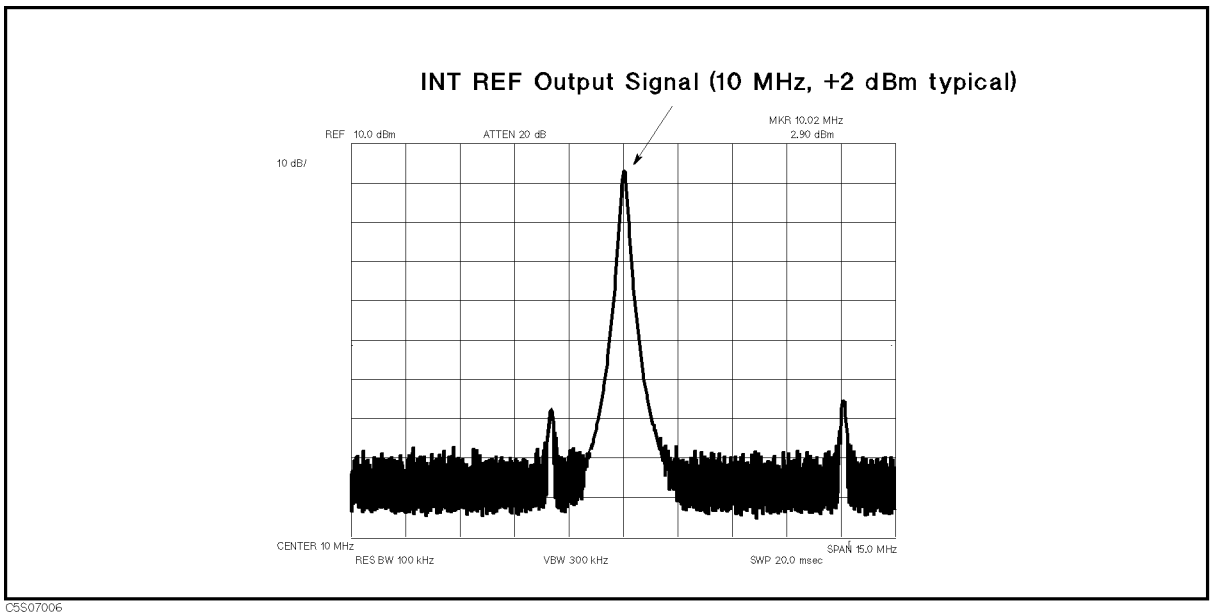

Figure 7-3. Typical INT REF Signal

2. Check the FRAC N OSC Signal

The fractional N oscillator (FRAC N OSC) generates the signal for frequencies from 31.25 MHz to 62.5 MHz. The signal level must be +4.5 dBm ± 5 dB over the frequency range. Perform the following steps to verify the frequency and level of the FRAC N OSC signal:

a. Press the following keys to monitor the FRAC N OSC frequency by using the bus measurement function:

(Preset), (System), SERVICE MENU, SERVICE MODES, BUS MEAS [OFF], FREQ BUS [OFF], (4), (x1), BUS MEAS on OFF (then the label changes to BUS MEAS ON off)

b. Make the sweep list of 1 MHz, 500 MHz, and 1 GHz as follows:

(Sweep Setup), ADD, (5), (0), (0), (M/μ), SEGMENT DONE, ADD, (1), (G/n), SEGMENT DONE, LIST DONE

c. Confirm that the FRAC N OSC frequency monitor value in the "X :" field is 2.0113 U ± 0.01 U at 1 MHz, 2.4986 U ± 0.01 U at 500 MHz, and 2.9869 U ± 0.01 U at 1 GHz.

Note

The FRAC N OSC frequency monitor value is calculated as (f+2058.58)/(16×16×4) [U], where *f* is the HP 4286A frequency setting [MHz].

- If the monitor readings are good, continue with the next step.
- If one (or more) of the monitor readings is bad, the FRAC N OSC is probably faulty. Replace A5.

d. Remove the "H" cable from the A5J7 "FN OUT" connector. Then connect the equipment as shown in Figure 7-4.

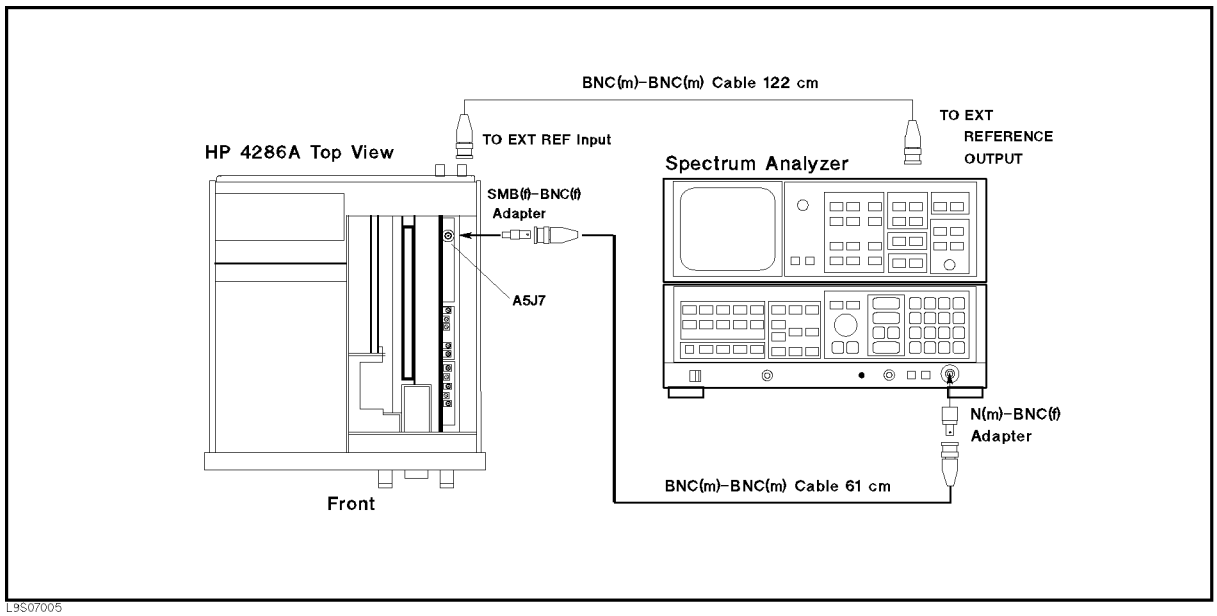

Figure 7-4. FRAC N OSC Signal Level Test Setup

e. On the HP 4286A, press (Preset), (Sweep Setup), EDIT, FREQ, (1), (M/μ), SEGMENT DONE, LIST DONE to set the HP 4286A frequency to 1 MHz.

f. Initialize the spectrum analyzer. Then set the controls as follows: (The sweep time must be less than 24 msec.)

Controls	**Settings**
Start Frequency	30 MHz
Stop Frequency	70 MHz
Reference Level	10 dBm

g. Check that the signal level is +4.5 dBm ± 5 dB at 32.18 MHz.

h. In the same manner, set the HP 4286A frequency to 500 MHz and 1 GHz. Then confirm that the signal level is +4.5 dBm ± 5 dB at 39.98 MHz and 47.79 MHz.

- If the signal is good, the FRAC N OSC is working. Continue with the next step.
- If the signal is bad, the FRAC N OSC is faulty. Replace A5.

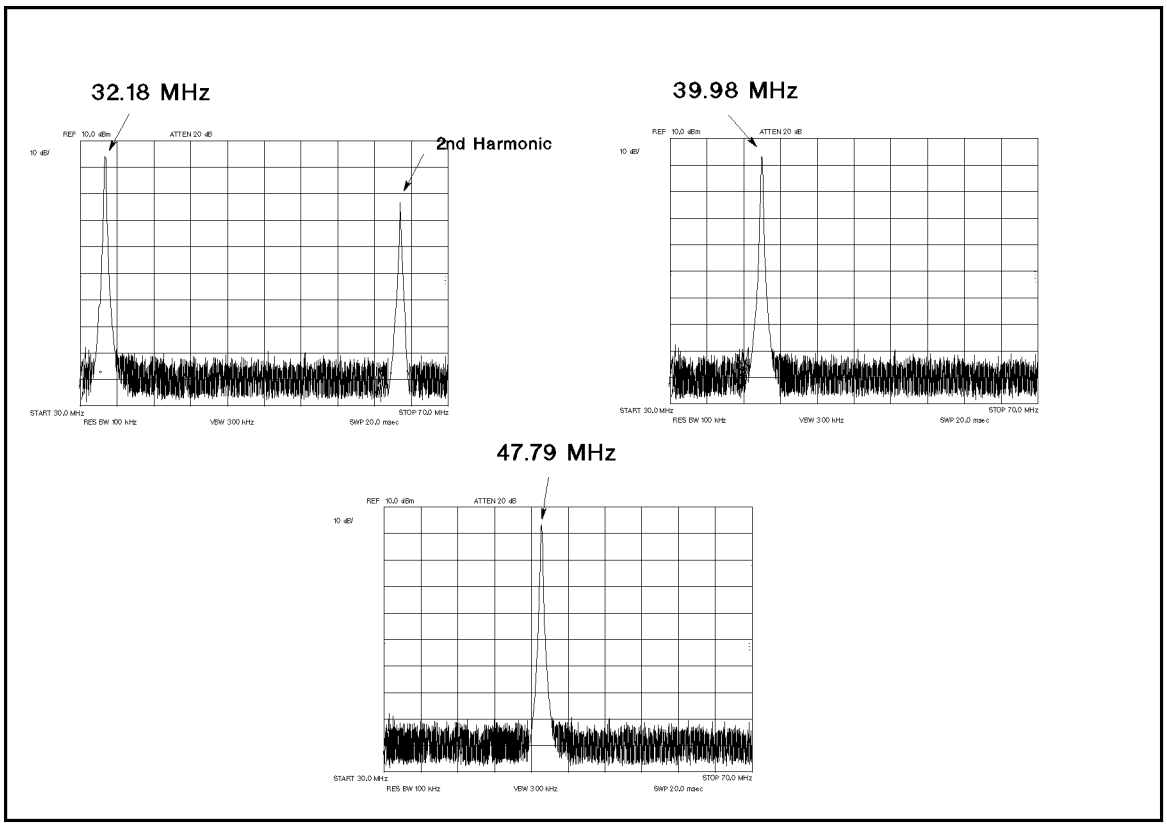

Figure 7-5. FRAC N OSC Typical Signal

i. Reconnect the "H" cable to the A5J7 "FN OUT" connector. Continue with *3. Check the 520 MHz Signal.*

3. Check the 520 MHz Signal

The 520 MHz signal (520 MHz, −15 dBm ± 0.2 dB) is derived from the 40 MHz reference signal through the ×13 Multiplier. See the A5 Synthesizer block in Figure 7-1. Therefore, the signal contains 40 MHz harmonics as shown in Figure 7-6. Perform the following steps to verify the 520 MHz signal:

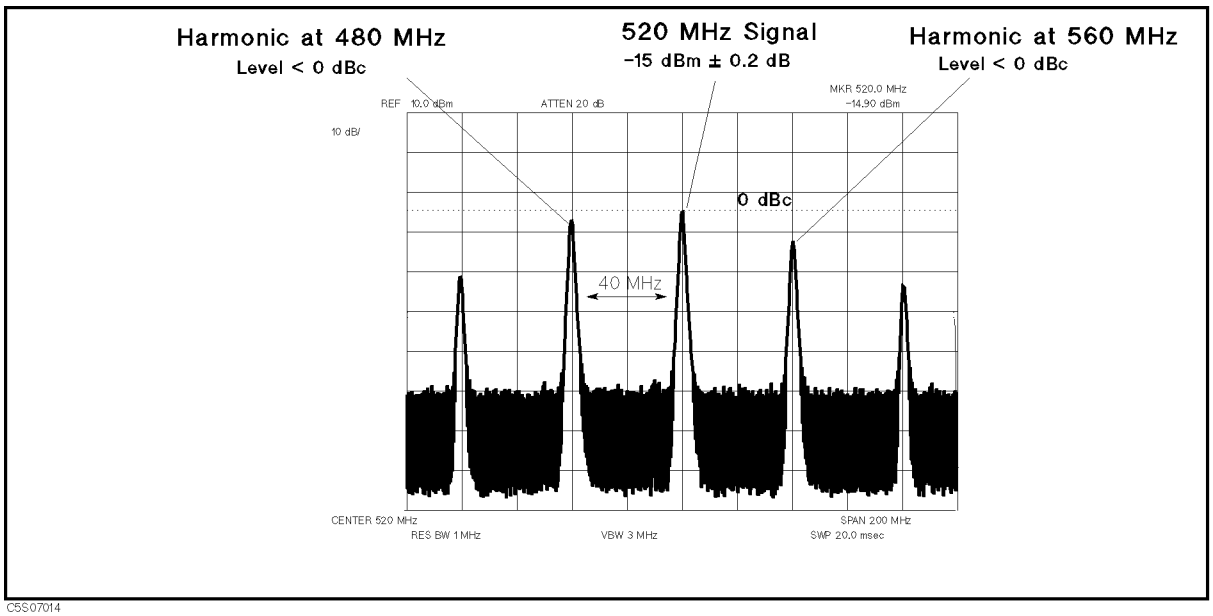

Figure 7-6. Typical 520 MHz Signal

a. Press (Preset) to initialize the HP 4286A.

b. Remove the "J" cable from the A5J3 "520 MHz OUT" connector. After the "PHASE LOCK LOOP UNLOCKED" message appears, connect the equipment as shown in Figure 7-7.

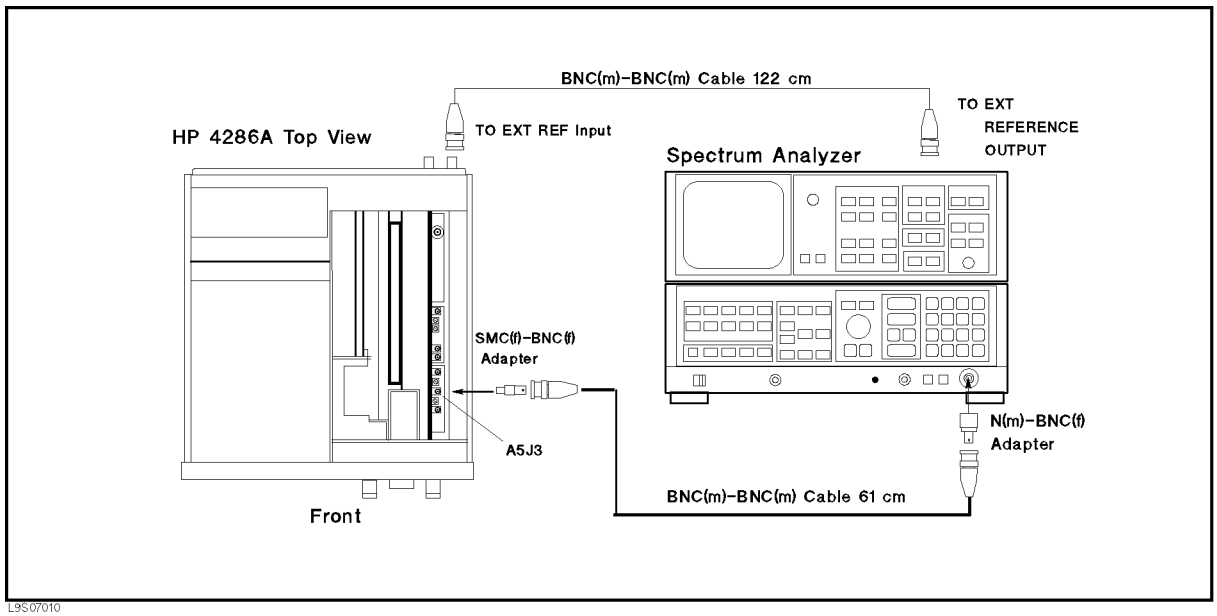

Figure 7-7. 520 MHz Signal Test Setup

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	**Settings**
Center Frequency	520 MHz
Span	200 MHz

d. On the spectrum analyzer, press (PEAK SEARCH) to move the marker to the peak of the 520 MHz signal.

e. Check that the frequency is 520 MHz, the level is -15 dBm ± 0.2 dB, and the harmonic levels at 480 MHz and 560 MHz are lower than 0 dBc (lower than the 520 MHz signal level). The trace displayed on the spectrum analyzer should be as shown in Figure 7-7.

- If the signal is good, continue with *4. Check the EXT REF Operation.*
- If the signal level is out of the limits, perform the *520 MHz Level Adjustment* (see Chapter 3).
  - If the adjustment is successfully completed, continue with *4. Check the EXT REF Operation.*
  - If the adjustment fails, the ×13 multiplier is faulty. Replace A5.
- If the signal is bad, the ×13 multiplier is faulty. Replace A5.

4. Check the EXT REF Operation

When an external reference signal (10 MHz, 0 dBm) is applied to the EXT REF input connector on the rear panel, the message "`ExtRef`" appears on the display. When the external reference signal is removed, the "`ExtRef`" message disappears.

Perform the following steps to verify the operation of the EXT REF input:

a. Connect the equipment as shown in Figure 7-8. Then check that the "`ExtRef`" message appears on the display.

b. Disconnect the cable from the EXT REF input. Then check that the "`ExtRef`" message disappears.

- If the "`ExtRef`" message appears and disappears correctly, the EXT REF circuit probably working. At this point, the A5 synthesizer is verified.
- If the "`ExtRef`" message does not appear, inspect the cable and connections between the EXT REF input connector and A5J4. See Figure 7-9 for the A5J4 location. If the cable and connections are good, the most probable faulty assembly is A5. Replace A5.

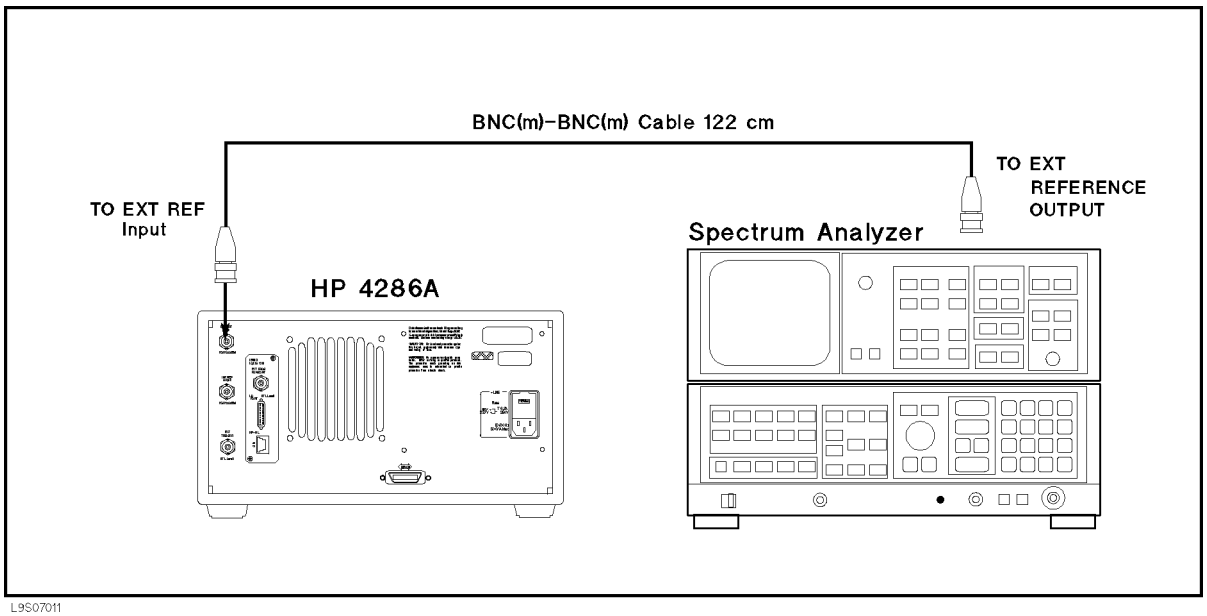

Figure 7-8. EXT REF Test Setup

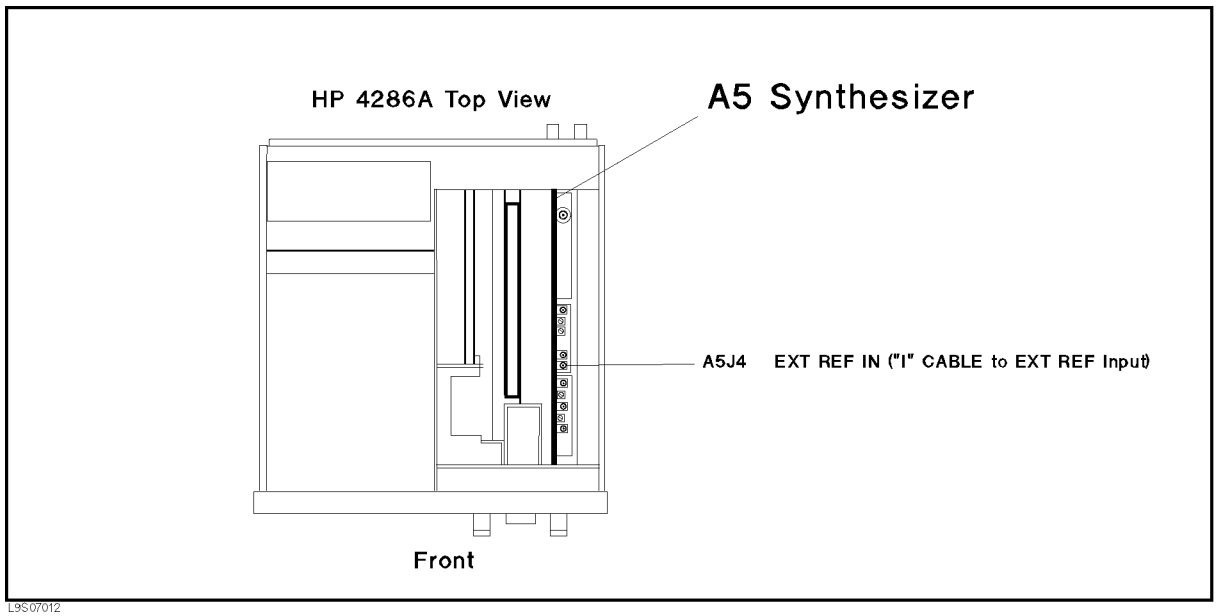

Figure 7-9. A5J4 Location

CHECK A4A1 1ST LO OUTPUTS

The input signal to A4A1 is the FRAC N OSC signal (see Figure 7-1). Before performing the procedures in this section, verify the FRAC N OSC signal in accordance with the previous section.

The output signals from A4A1 are two 1st local oscillator signals (2.05958 GHz to 3.05858 GHz). One goes from the A4A1J3 connector to the A3A3 source. The other goes from the A4A1J4 connector to the A4A2 Receiver RF. If the two signals are good, the A4A1 1st LO is verified.

Perform the following procedures sequentially to verify the two A4A1 output signals at A4A1J3 and A4A1J4.

Note If one or both of the signals are bad, the A4A1 1st LO is faulty. Replace the A4 1st LO/Receiver RF (which consists of the A4A1 1st LO and the A4A2 Receiver RF).

1. Check the 1st LO OSC Signal at A4A1J3

The 1st local oscillator signal at A4A1J3 is the 2.05958 GHz to 3.05858 GHz signal with the power level between -13 dBm to -3 dBm over the frequency range. Perform the following steps to verify the 1st local oscillator signal at A4A1J3:

a. Remove the "C" semi-rigid cable from A4A1J3, and connect the equipment as shown in Figure 7-10. In this procedure, connect the spectrum anlyzer input to A4A1J3.

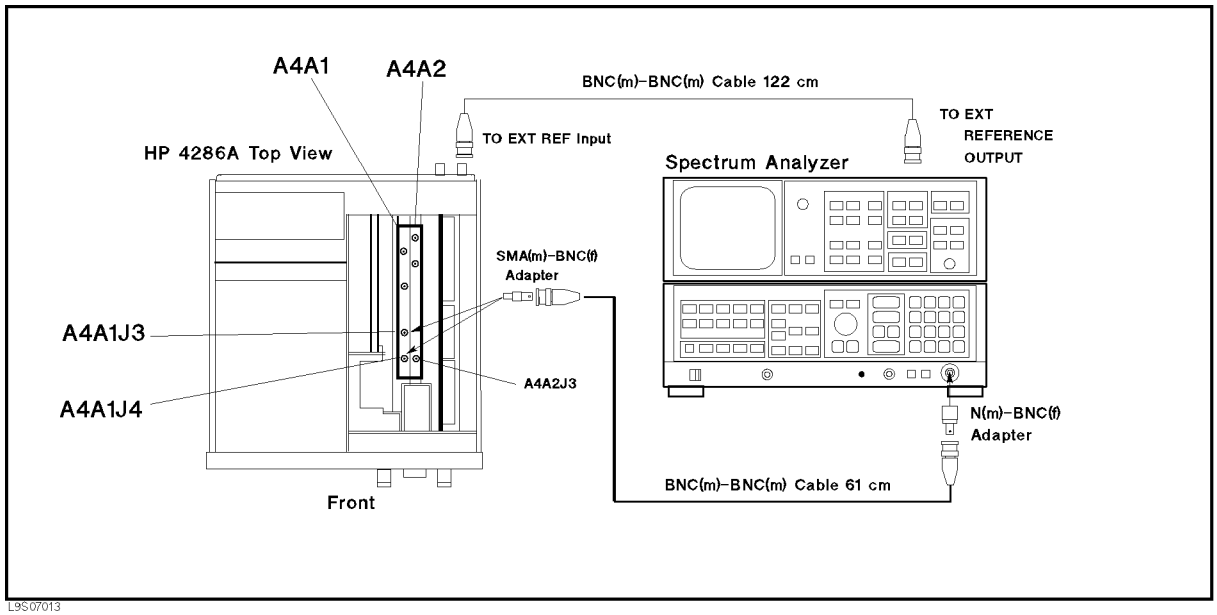

Figure 7-10. 1st LO OSC Signal Test Setup

b. Press (Preset), (Sweep Setup), EDIT, FREQ, (1), (M/μ), SEGMENT DONE, LIST DONE to set the HP 4286A frequency to 1 MHz.

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	Settings
Start Frequency	2 GHz
Stop Frequency	4 GHz
Reference Level	0 dBm

d. Check that the signal level is -13 dBm to -3 dBm at 2.05958 GHz.

e. In the same manner, set the HP 4286A frequency to 500 MHz and 1 GHz. Then check that the signal level is -13 dBm to -3 dBm at 2.55858 GHz and 3.05858 GHz.

Note

The measured level is lower than the actual level due to the BNC(m)-BNC(m) cable's insertion loss at high frequencies. If the measured level is lower than the limit, measure the cable's loss and compensate the signal level by the cable's loss.

- If the signal level and the trace are good, continue with the next step.
- If the signal level or the trace is bad, the A4A1 1st LO is faulty. Replace A4.

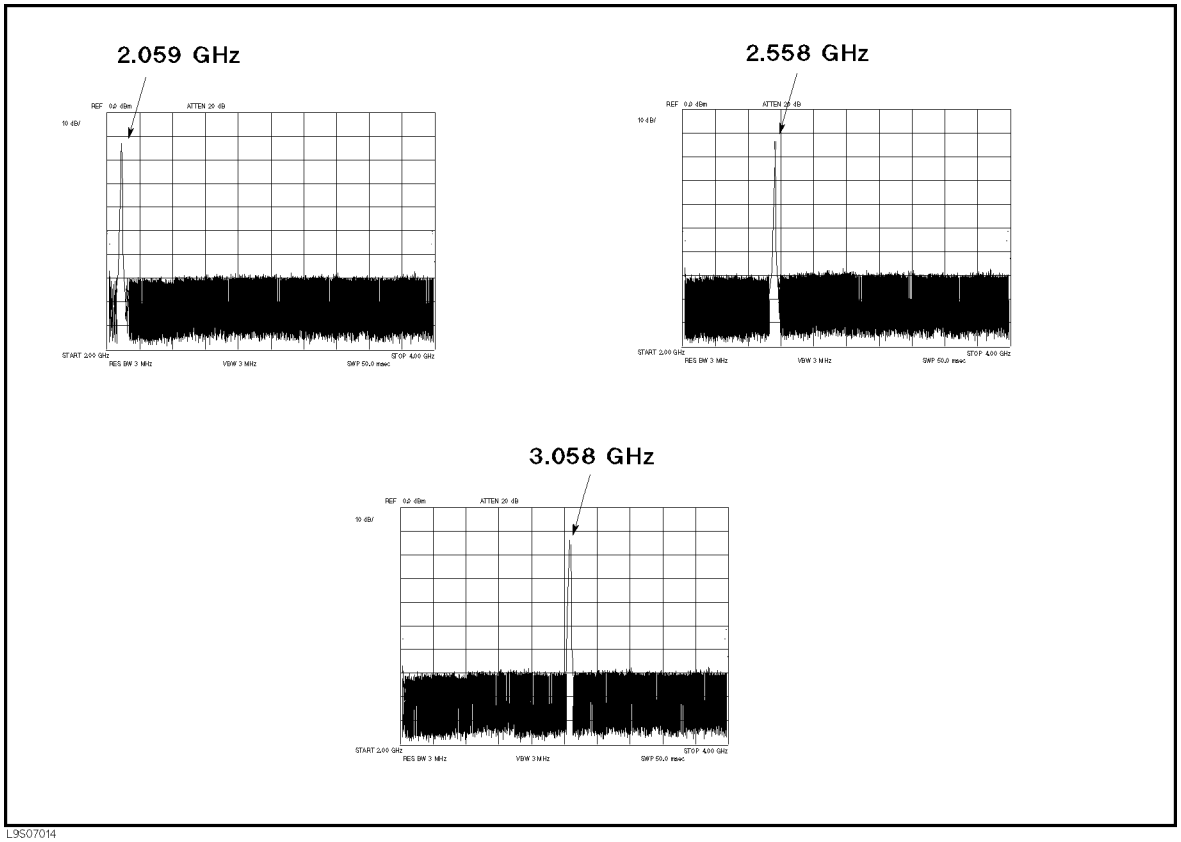

Figure 7-11. Typical 1st LO OSC Signal (Single Mode) at A4A1J3

2. Check the 1st LO OSC Signal at A4A1J4

The 1st local oscillator signal at A4A1J4 is the 2.05958 GHz to 3.05858 GHz signal with the power level > +16 dBm over the frequency range. Perform the following steps to verify the 1st local signal at A4A1J4:

a. Remove the "F" semi-rigid cable from A4A1J4 and A4A2J3, and connect the eqiupment as shown in Figure 7-10. In this procedure, connect the spectrum analyzer input to A4A1J4.

b. Press (Preset), (Sweep Setup), EDIT, FREQ, (1), (M/μ), SEGMENT DONE, LIST DONE to set the HP 4286A frequency to 1 MHz.

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	**Settings**
Start Frequency	2 GHz
Stop Frequency	4 GHz
Reference Level	20 dBm

d. Check that the signal level is higher than +16 dBm at 2.05958 GHz.

e. In the same manner, set the HP 4286A frequency to 500 MHz and 1 GHz. Then check that the signal level is higher than +16 dBm at 2.55858 GHz and 3.05858 GHz..

The measured level is lower than the actual level due to the BNC(m)-BNC(m) cable's insertion loss in the high frequency range. If the measured level is lower than the limit, measure the cable's loss and compensate the signal level by the cable's loss.

- If the signal level and the trace are good, continue with the next step.
- If the signal level or the trace is bad, the A4A1 1st LO is faulty. Replace A4.

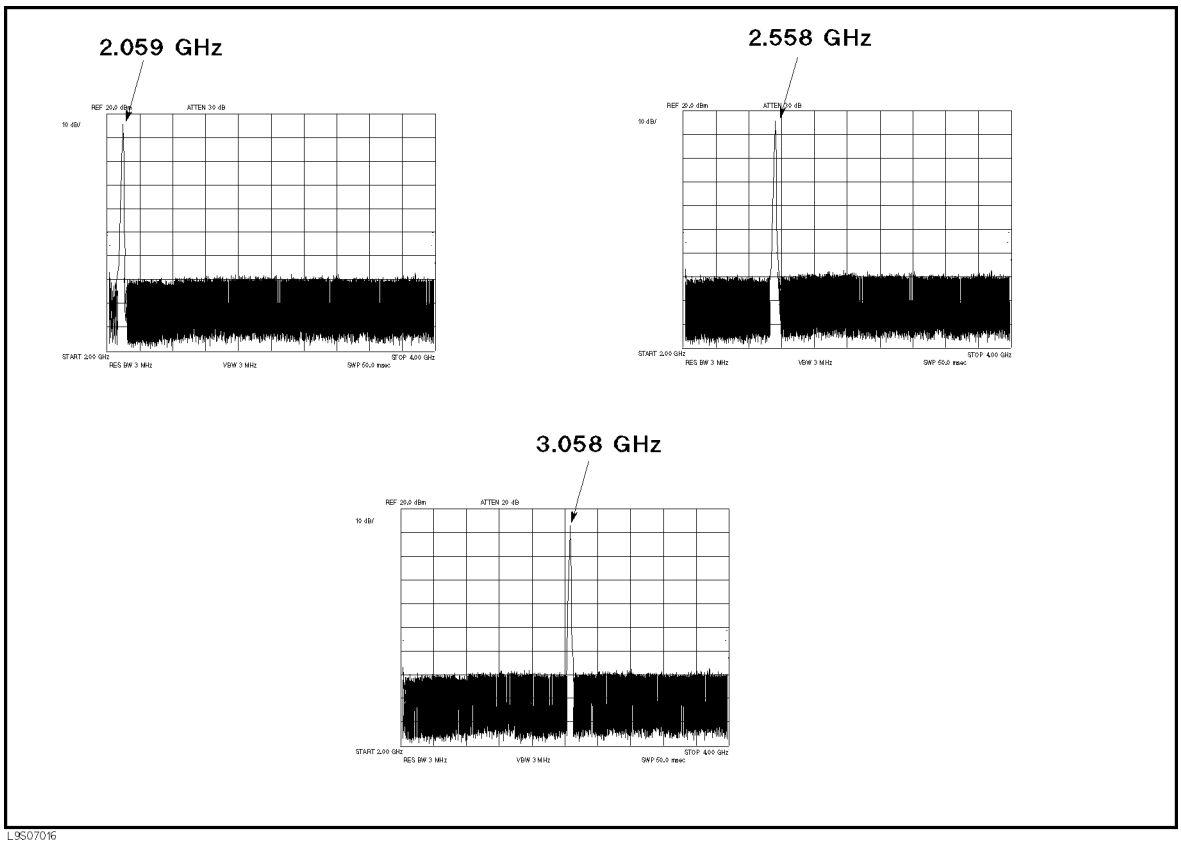

Figure 7-12. 1st LO OSC Typical Signal (Single Mode) at A4J4

f. Reconnect the "F" semi-rigid cable to A4A1J4 and A4A2J3. At this point, the A4A1 1st LO is verified.

CHECK A3A1 SOURCE VERNIER OUTPUT

The input signal to the A3A1 Source Vernier is the 40 MHz reference signal coming from A5 (see Figure 7-1). Before performing the procedures in this section, verify the INT REF signal in accordance with the *Check A5 Synthesizer Outputs* section. This ensures that the 40 MHz reference signal is good.

The three output signals from A3A1 are the 21.42 MHz signal with the level controlled by the level vernier, the 8 MHz reference signal, and the 40 kHz reference signal.

Perform the following procedures sequentially to verify the 21.42 MHz signal. If the signal is bad, replace A3A1.

In this procedure, only the 21.42 MHz signal is verified. This is because the 8 MHz and 40 kHz reference signals are verified by running internal test 10 in the *Start Here*.

The 21.42 MHz signal is observed using test equipment and its level is controlled by the HP 4286A self-test functions. For detailed information about the HP 4286A self-test functions, see the *Service Key Menus*.

1. Check the 21.42 MHz Signal

Perform the following steps to verify the 21.42 MHz signal:

a. Remove the "D" cable from A3A2J22, and connect the equipment as shown in Figure 7-13.

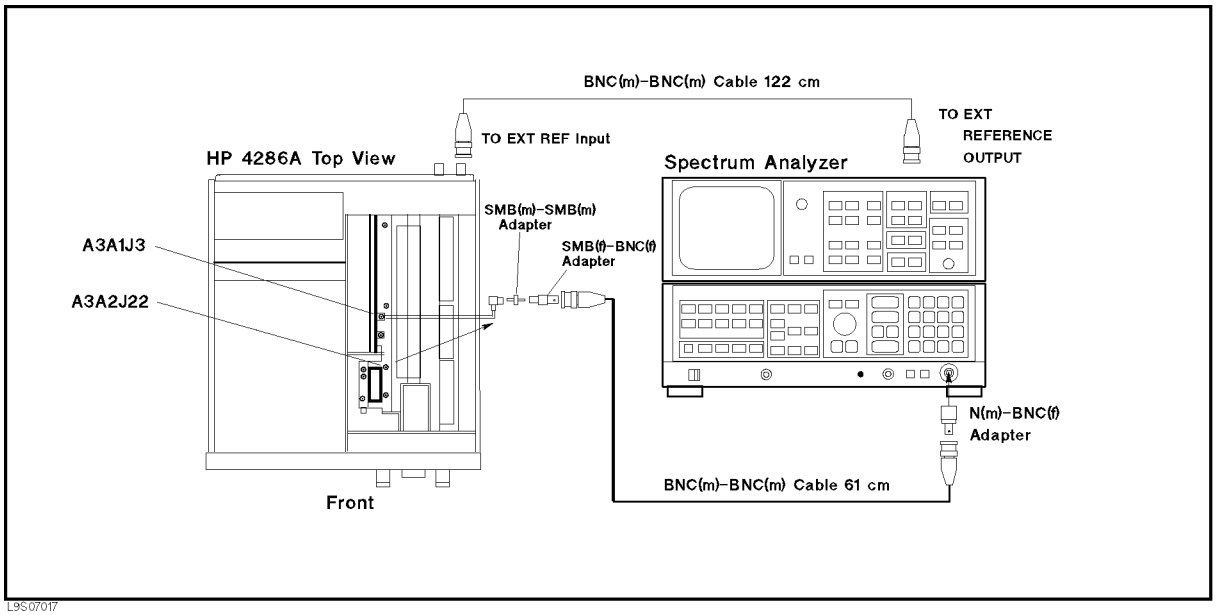

Figure 7-13. 21.42 MHz Signal Test Setup

b. Press [Preset] to initialize the HP 4286A.

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	Settings
Center Frequency	21.42 MHz
Span	1 MHz
Reference Level	10 dBm

d. On the HP 4286A, press the following keys to set the OSC DAC value to 13,000.

(System), SERVICE MENU, SERVICE MODES, OSC, OSC AUTO man (then the label changes to OSC auto MAN), OSC DAC AUTO man (then the label changes to OSC DAC auto MAN), OSC DAC VALUE, (1), (3), (0), (0), (0), (x1)

e. On the spectrum analyzer, press (PEAK SEARC) to move the marker to the peak of the 21.42 MHz signal.

f. Check that the frequency is 21.42 MHz and the level is higher than -18 dBm. The displayed trace should be as shown in Figure 7-14.

- If the signal is good, A3A1 is verified.
- If the signal is bad, replace A3A1.

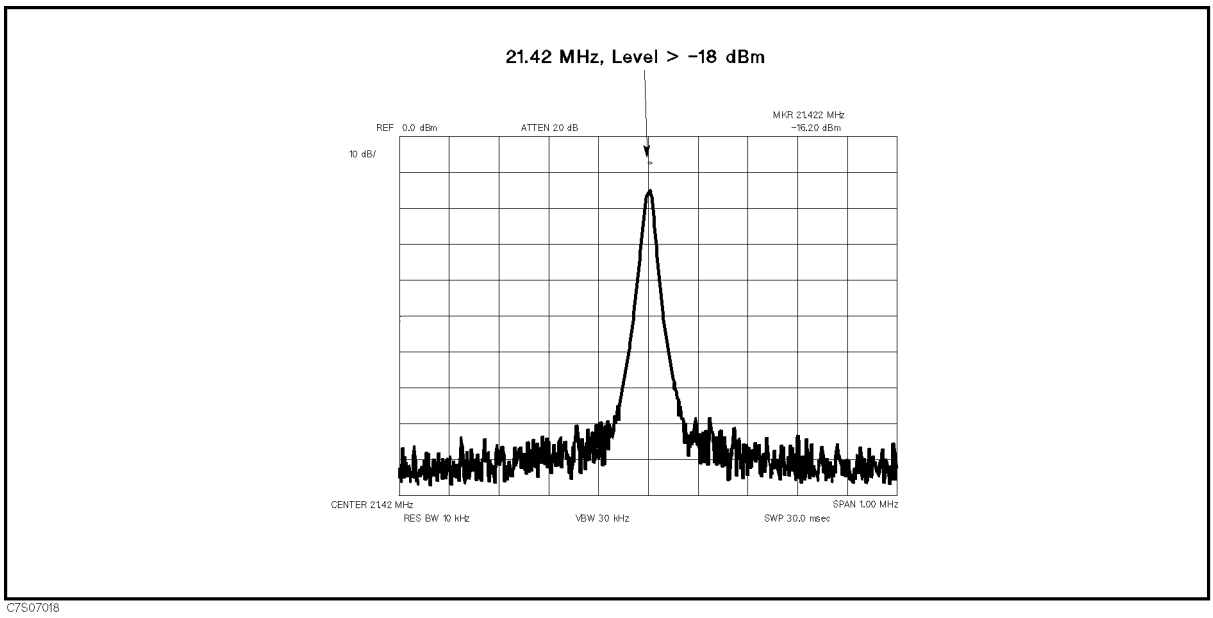

Figure 7-14. Typical 21.42 MHz Signal

CHECK A3A2 2ND LO OUTPUTS

The two input signals to A3A2 are the 520 MHz signal coming from A5 and the 21.42 MHz signal coming from A3A1. See Figure 7-1. Before performing the procedures in this section, verify the 520 MHz signal in accordance with the *Check A5 Synthesizer Outputs* section and verify the 21.42 MHz signal in accordance with the *Check an A3A1 Source Vernier Output* section.

The two output signals from A3A2 are the 2.08 GHz 2nd local oscillator signal going to the A4A2 Receiver IF and the 2.05858 GHz signal going to the A3A3 source. Perform the following procedures sequentially to verify these signals. If one of the signals is bad, replace A3A2.

In this procedure, the 2.05858 GHz signal level is controlled by the HP 4286A self-test functions. For detailed information about the HP 4286A self-test functions, see the *Service Key Menus*.

1. Check the 2nd Local Oscillator Signal

The 2nd local oscillator signal is the 2.08 GHz CW signal a with signal level > +7 dBm (typical). Perform the following steps to verify the frequency and level of the 2nd local oscillator signal:

a. Remove the "I" semi-rigid cable from A3A2J19 and remove the "D" cable from A3A1J3. See Figure 7-15 for the locations of A3A2J19 and A3A1J3. Then connect the equipment as shown in Figure 7-15.

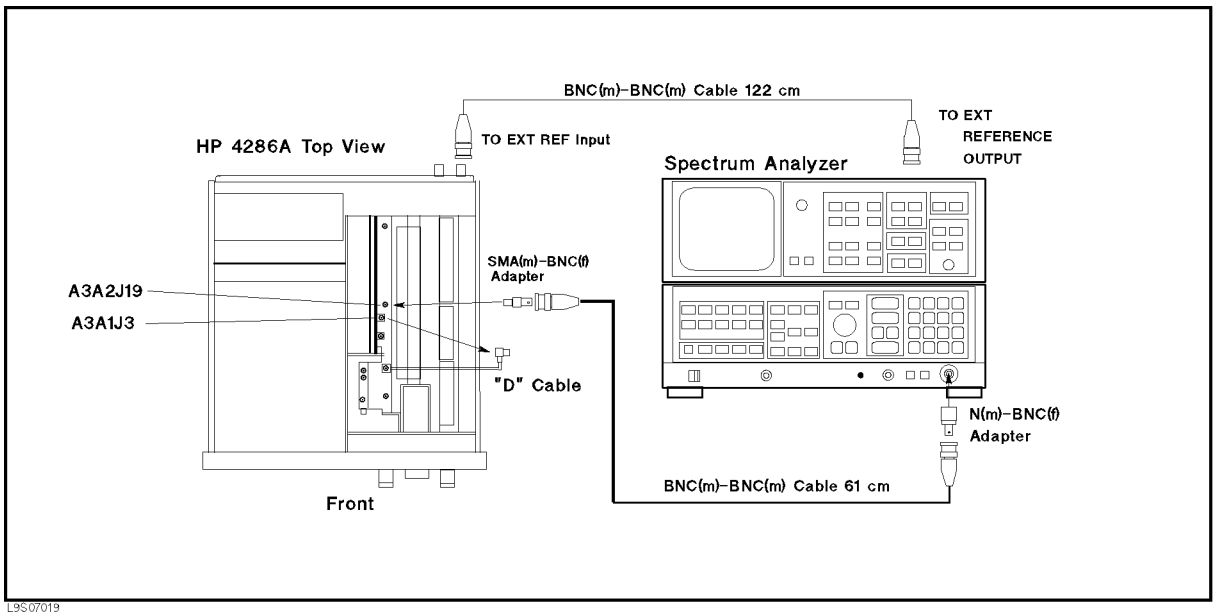

Figure 7-15. 2nd LO OSC Test Setup

b. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	Settings
Center Frequency	2.08 GHz
Span	1 MHz
Reference Level	20 dBm

c. On the spectrum analyzer, press (PEAK SEARCH) to move the marker to the peak of the 2nd Local.

d. Check that the frequency is 2.08 GHz and the level is higher than +7 dBm. The 2nd local oscillator signal should be as shown in Figure 7-16.

The measured level is lower than the actual level due to the BNC(m)-BNC(m) cable's insertion loss at high frequency. If the measured level is lower than the limit, measure the cable's loss and compensate the signal level by the cable's loss.

- If the signal is good, continue with the next step.
- If it is bad, perform the *Second Local PLL Lock Adjustment* (see Chapter 3). If the problem persists after the adjustment, the A3A2 2nd LO OSC is faulty. Replace A3A2.

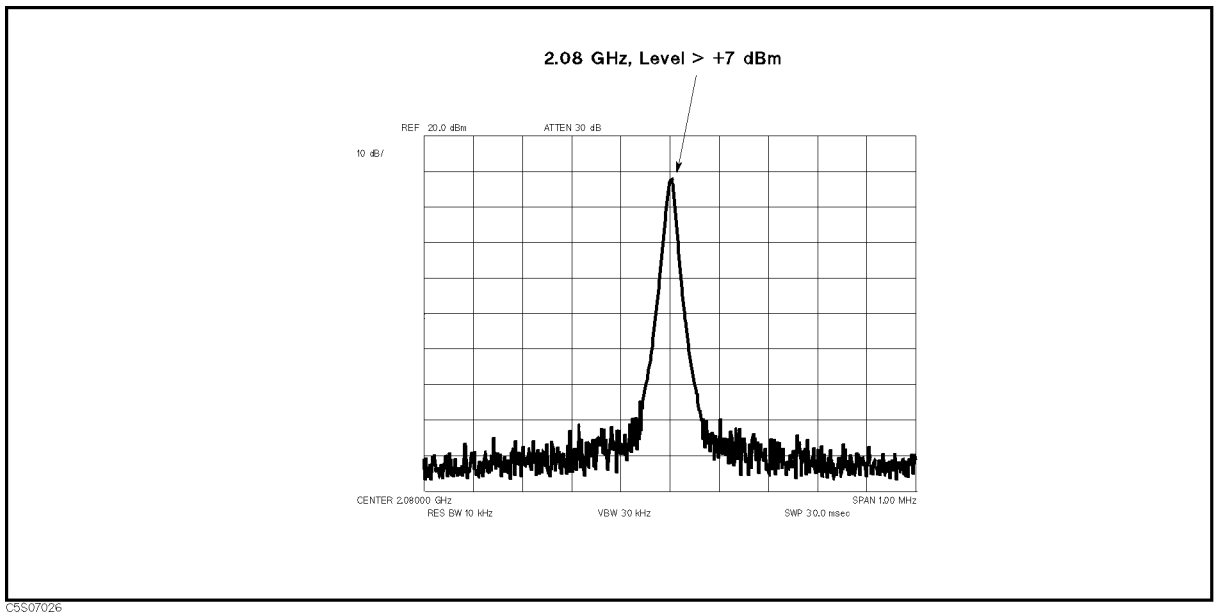

Figure 7-16. Typical 2nd Local Oscillator Signal

e. Reconnect the "I" semi-rigid cable to A3A2J19 and reconnect the "D" cable to A3A1J3. Then continue with *2. Check the 2.05858 GHz Signal.*

2. Check the 2.05858 GHz Signal

The 2.05858 GHz signal level is controlled by the ALC loop. See the A3A2 2nd LO block in Figure 7-1. Perform the following steps to verify the frequency and level of the 2.05858 GHz signal:

a. Remove the "E" cable from A3A2J23. See Figure 7-17 for the location of A3A2J23. Then connect the equipment as shown in Figure 7-17.

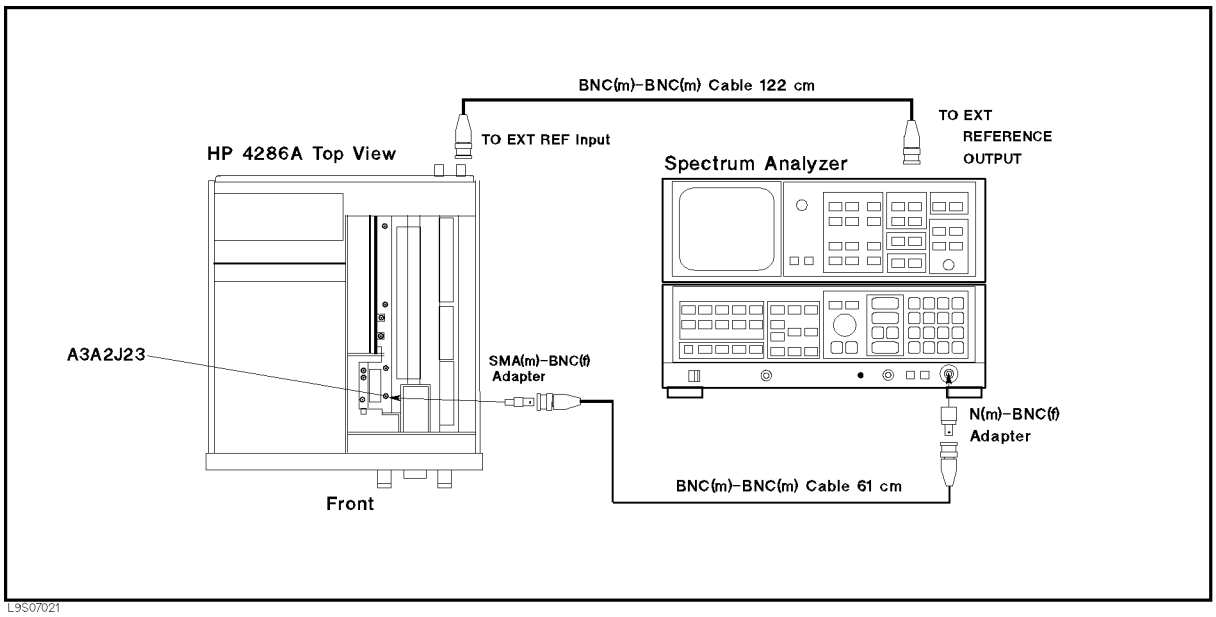

Figure 7-17. 2.05858 GHz Signal Test Setup

b. Press (Preset) to initialize the HP 4286A.

c. Initialize the spectrum analyzer. Then set the controls as follows:

Controls	Settings
Center Frequency	2.05858 GHz
Span	1 MHz
Reference Level	20 dBm

d. On the HP 4286A, press the following keys to set the OSC level control DAC value to 13,000.

(System), SERVICE MENU, SERVICE MODES, OSC, OSC AUTO man (then the label changes to OSC auto MAN), OSC DAC AUTO man (then the label changes to OSC DAC auto MAN), OSC DAC VALUE, (1), (3), (0), (0), (0), (x1)

e. On the spectrum analyzer, press (PEAK SEARCH) to move the marker to the peak of the ALC output signal.

f. Check that the frequency is 2.05858 GHz and the level is higher than -13 dBm. The displayed trace should be as shown in Figure 7-18.

- If the signal is good, continue with the next step.
- If the signal is bad, the Source First Mixer is faulty. Replace A3A2.

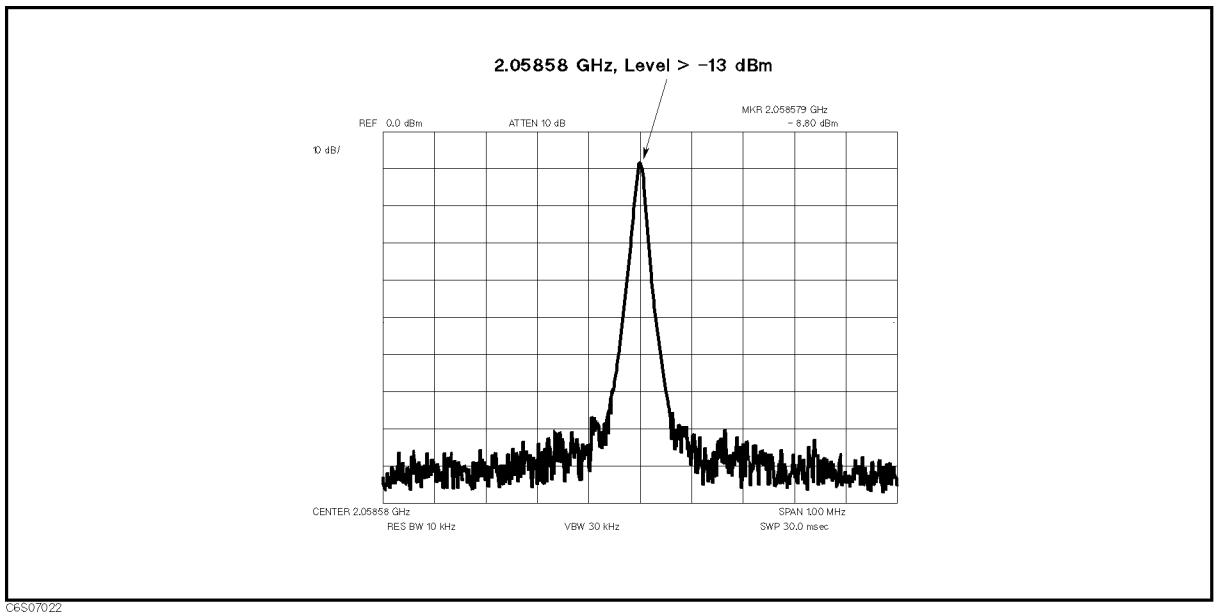

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Figure 7-18. Typical 2.05858 GHz Signal

g. Reconnect the “E” semi-rigid cable to A3A2J23. At this point, the A3A2 2nd LO is verified.

CHECK A3A3 SOURCE OUTPUT

The two input signals to A3A3 are the 1st local oscillator signal coming from A4A1 and the 2.05858 GHz signal coming from A3A2. See Figure 7-1. Before performing the procedures in this section, verify the 1st local oscillator signal at A4A1J3 in accordance with the *Check A4A1 1st LO Outputs* section and verify the 2.05858 GHz signal in accordance with the *Check A1A2 2nd LO Outputs*.

The two output signals from A3A3 are the RF signal (1 MHz to 1 GHz, -10 dBm to +20 dBm) going to the A7 output attenuator and the level detector's signal going to the A3A1 Source Vernier. Only the RF signal is checked in the following procedure, because the level detector's signal are already verified in the internal test 14: SOURCE LEVEL.

Perform the following procedure to verify the RF signal.

1. Check the A3A3 RF Signal

The A3A3 source generates the RF signal (1 MHz to 1 GHz). Perform the following steps to verify the frequency and level of the RF signal:

a. Connect the power sensor to the power meter, and calibrate the power meter for the power sensor.

b. Connect the equipment as shown in Figure 7-19.

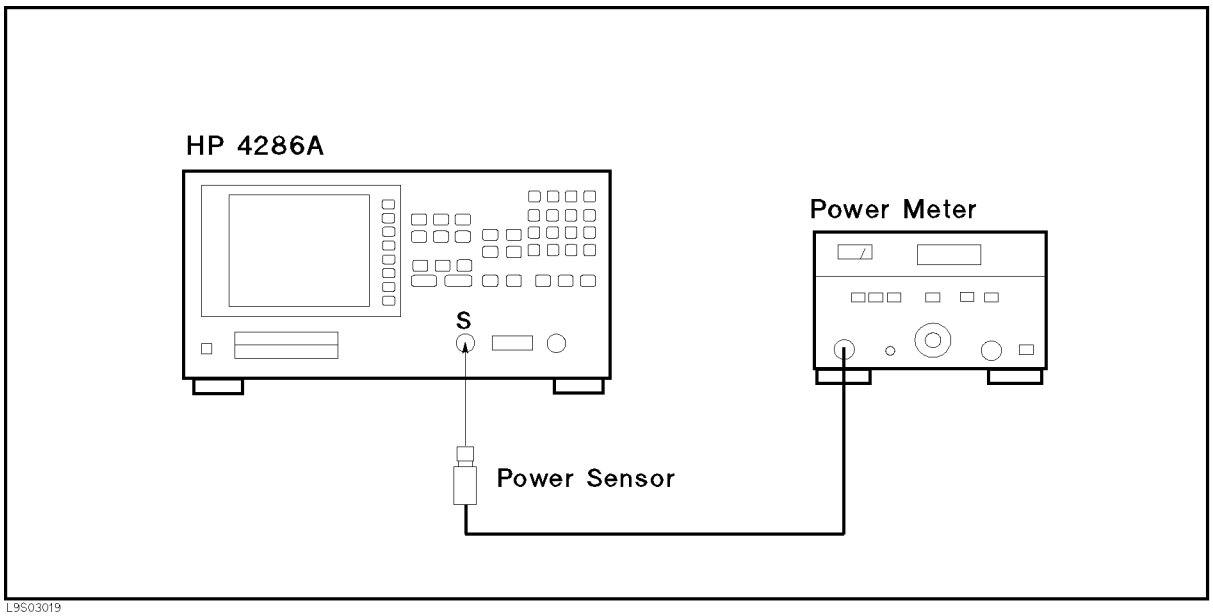

Figure 7-19. A3A3 RF Signal Test Setup

c. Press the following keys to set the first setting of the RF signal test. (Preset), (System), `Service Menu`, `Service Modes`, `OSC`, `OSC AUTO man` (then the label changes to `OSC auto MAN`), `OUTPUT ATT [AUTO]`, `0 dB`, {then the label changes to `OUTPUT ATT [0 dB]`, `OSC DAC AUTO man` (then the label changes to `OSC DAC auto MAN`), `OSC DAC VALUE`, (1), (0), (0), (0), (x1)

d. Check that the power meter readings are within the test limits under the conditions of Table 7-1.

- If the result is good, A3A3 is verified.
- If the result is bad, check the A3A3 output directly by disconnecting the semi-rigid cable "D" from A3A3.

  If the A3A3 output is bad, replace A3A3. If the A3A3 output is good, check the semi-rigid cable "D", the A7 output attenuator, and the flexible cable connected to the S connector.

Table 7-1. A3A3 RF Signal Test Settings

HP 4286A Frequency	Output ATT	OSC DAC	Test Limit
1 MHz	0 dB	1000	0 dBm ±6 dB
1 GHz	0 dB	3222	6 dBm ±6 dB
1 GHz	10 dB	32000	> 6.5 dBm

CHECK A7 OUTPUT ATTENUATOR CONTROL SIGNALS

Use this procedure when the A7 Output Attenuator is the most suspicious assembly (for example, if external test 19 fails).

A7 is controlled by the three signals at A7J1, A7J2, and A7J3 that come from the A2 post-regulator.

Perform the following procedure to verify the A7 control signals. If the signals are bad, replace A2.

In this procedure, the control signal is set using the HP 4286A self-test functions. For detailed information about the HP 4286A self-test functions, see the *Service Key Menus*.

1. Check A7 Control Signals

The A7 Output Attenuator is controlled by the three lines at A7J1, A7J2, and A7J3 as shown in Figure 7-19. Perform the following steps to verify the A7 control signals:

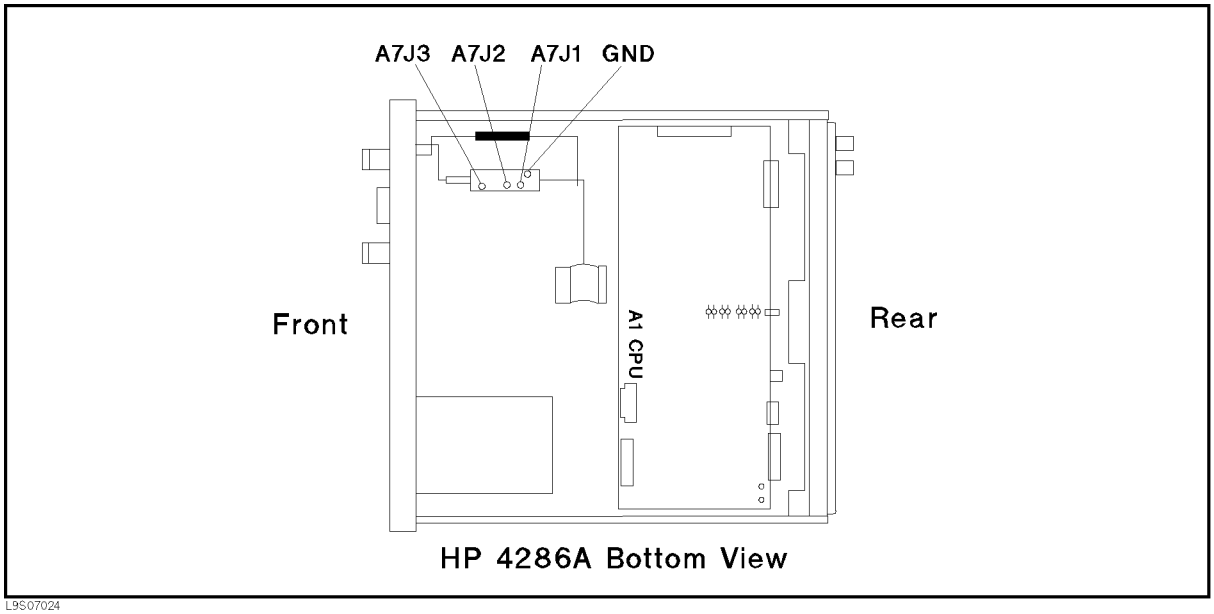

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Figure 7-20. A7 Output Attenuator Control Signals

a. Press the following keys to set the HP 4286A OSC level to manual mode.

(Preset), (System), `Service Menu`, `Service Modes`, `OSC`, `OSC AUTO man` (then the label changes to `OSC auto MAN`)

b. On the HP 4286A, press `OUTPUT ATT [AUTO]`, `0 dB` to set A7 to the first test setting of 0 dB in Table 7-2.

c. Measure voltage at A7J1, A7J2, and A7J3 using a voltmeter. Then check the measured values are within limits. The typical voltages are listed in Table 7-2.

- If the control voltages are good, continue with the next step.
- If the control voltages are bad, inspect the cable between A7 and A20J20. If the cable is good, the attenuator control circuit in the A2 post-regulator is probably faulty. Replace A2.

Table 7-2. A7 Attenuation Test Settings

A7 Attenuation	A7J1 Voltage	A7J2 Voltage	A7J3 Voltage
0 dB	High[1]	Low[2]	Low
−10 dB	Low	Low	Low
−20 dB	High	High	Low
−30 dB	High	Low	High
−40 dB	Low	Low	High
−50 dB	High	High	High
−60 dB	Low	High	High

1 Within +8.4 V to +16 V (+12 V typical)

2 0 V typical

d. Repeat steps b and c to set A7 in accordance with Table 7-2.

At this point, the A7 attenuator control signals are verified.

8

Receiver Group Troubleshooting

INTRODUCTION

Use these procedures only if you have read Chapter 4 and you believe the problem is in the receiver group.

This chapter provides procedures to isolate the faulty assembly in the receiver group.

The procedures isolate the faulty assembly by using the HP 4286A self-test functions (external tests). Remember that these tests are done on the assumption that the source group is operating correctly.

The receiver group consists of the following two assemblies:

- A4A2 Receiver RF (Part of A4 First LO/Receiver RF)
- A6 Receiver IF

Note

Make sure all of the assemblies listed above are firmly seated before performing the procedures in this chapter.

Allow the HP 4286A to warm up for at least 30 minutes before you perform any procedure in this chapter.

Figure 8-1 is a receiver group simplified block diagram. For more information about circuit operation, see Chapter 11.

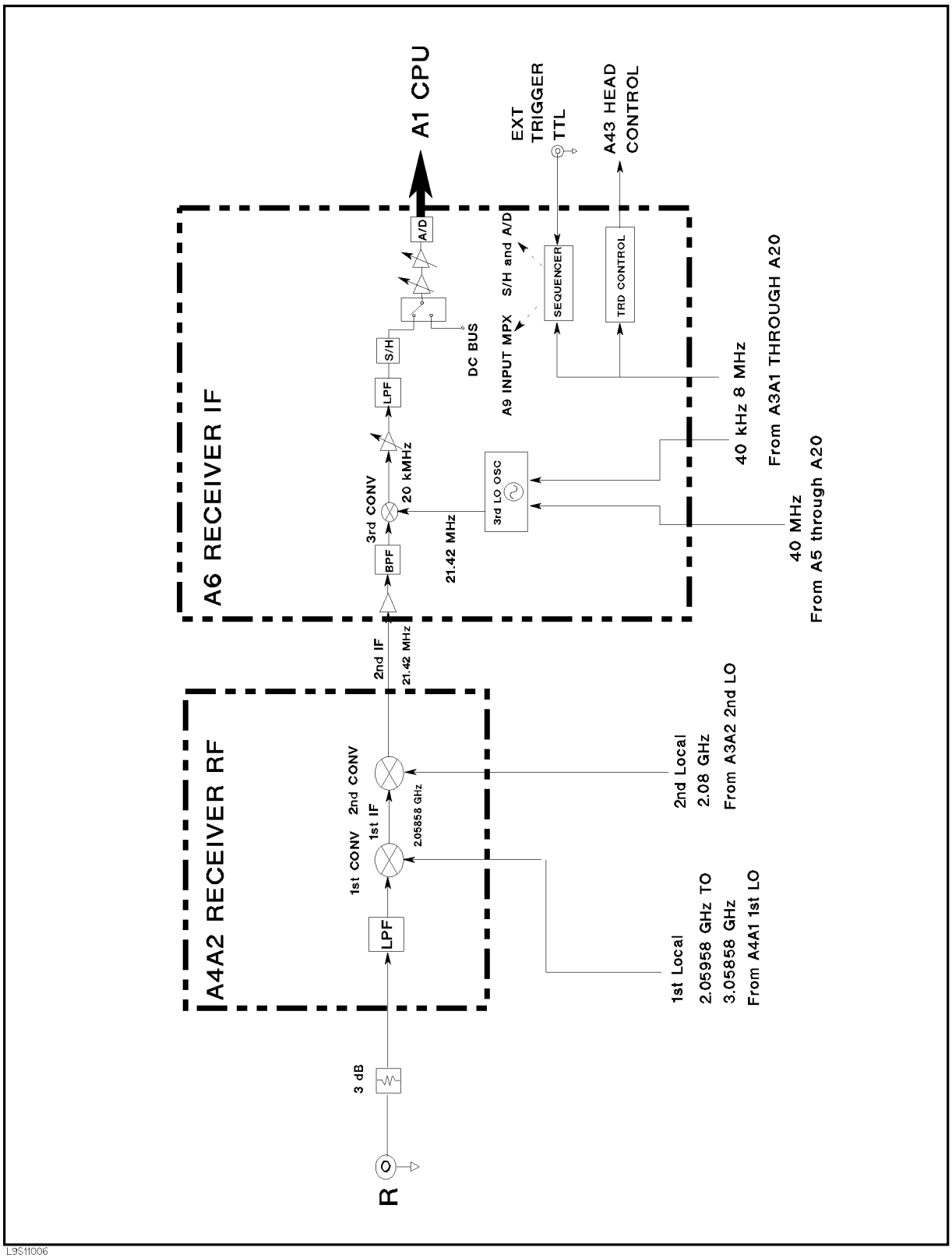

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Figure 8-1. Receiver Group Block Diagram

RECEIVER GROUP TROUBLESHOOTING SUMMARY

This section summarizes the sequence of troubleshooting in this chapter.

The receiver group troubleshooting flow is shown in Figure 8-2.

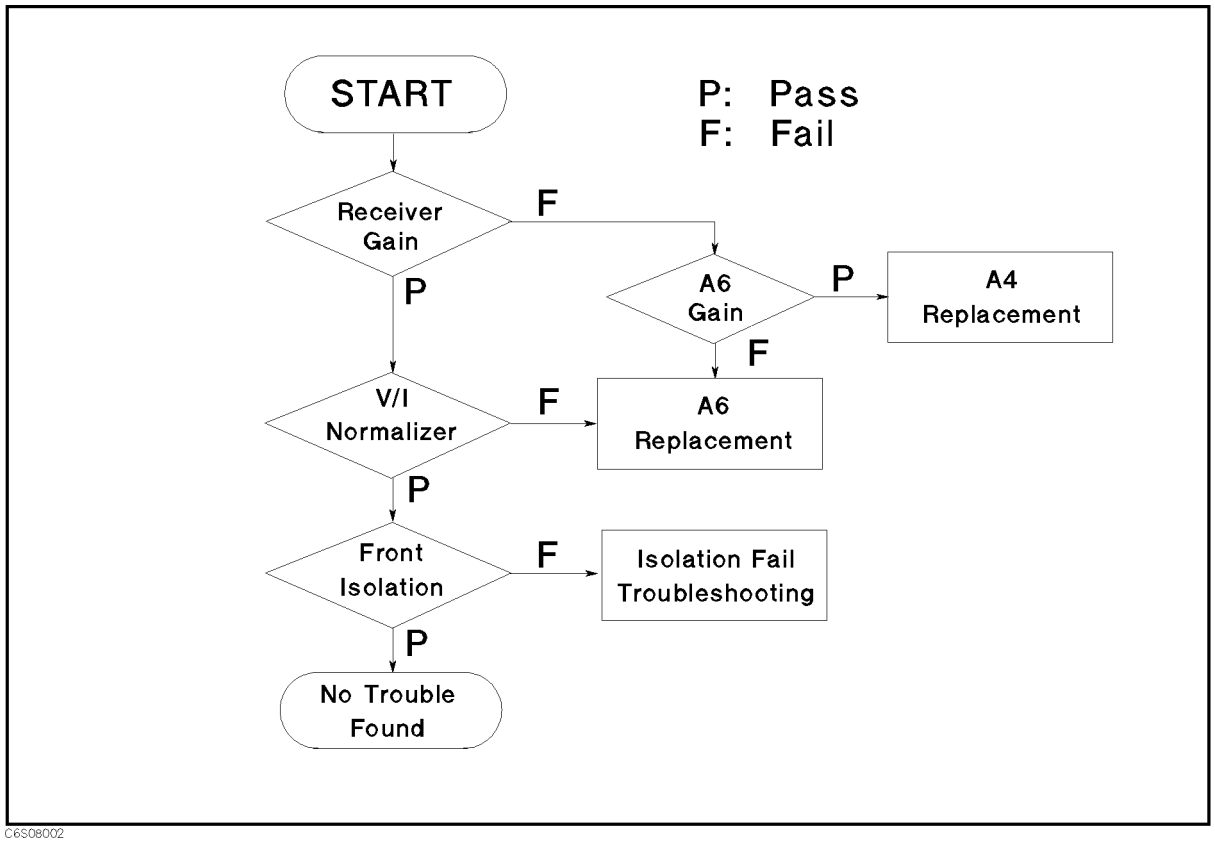

Figure 8-2. Receiver Group Troubleshooting Flow

Troubleshooting consists of two parts. The first part is to isolate the fault between the A4A2 receiver RF and A6 receiver IF. The second part is to verify signal isolation between the source circuits and the receiver circuits.

Fault isolation between A4A2 and A6 is done by using the following three self-tests:

Test Number	Description
20	RECEIVER GAIN
21	A6 GAIN
22	V/I NORMALIZER

After both the RECEIVER GAIN test and V/I NORMALIZER test pass, signal isolation between the source circuits and the receiver circuits is verified using the FRONT ISOL'N test. If the test passes, the receiver group is probably operating correctly.

START HERE

This section provides the step by step troubleshooting procedure using the HP 4286A self-test functions (external tests). For detailed information about the self-test functions, see Chapter 10.

Test Equipment

Type-N Cable, 61 cm .....HP 11500B or part of HP 11851B

Procedure

1. Press (Preset), (System), SERVICE MENUS, TESTS, (2), (0), (x1) to access the RECEIVER GAIN test. When "RECEIVER GAIN" is displayed, press EXECUTE TEST.
2. Perform the test according to the displayed instructions.
   - If the test passes, go to step 7.
   - If the test fails, continue with the next step.
3. Turn the HP 4286A power off. Remove the "D" cable from the A3A1 ALC out connector, remove the "M" cable from the A4A2 second IF connector, then connect the "M" cable to the A3A1 ALC out connector. The connecors locations are shown in Figure 8-3.

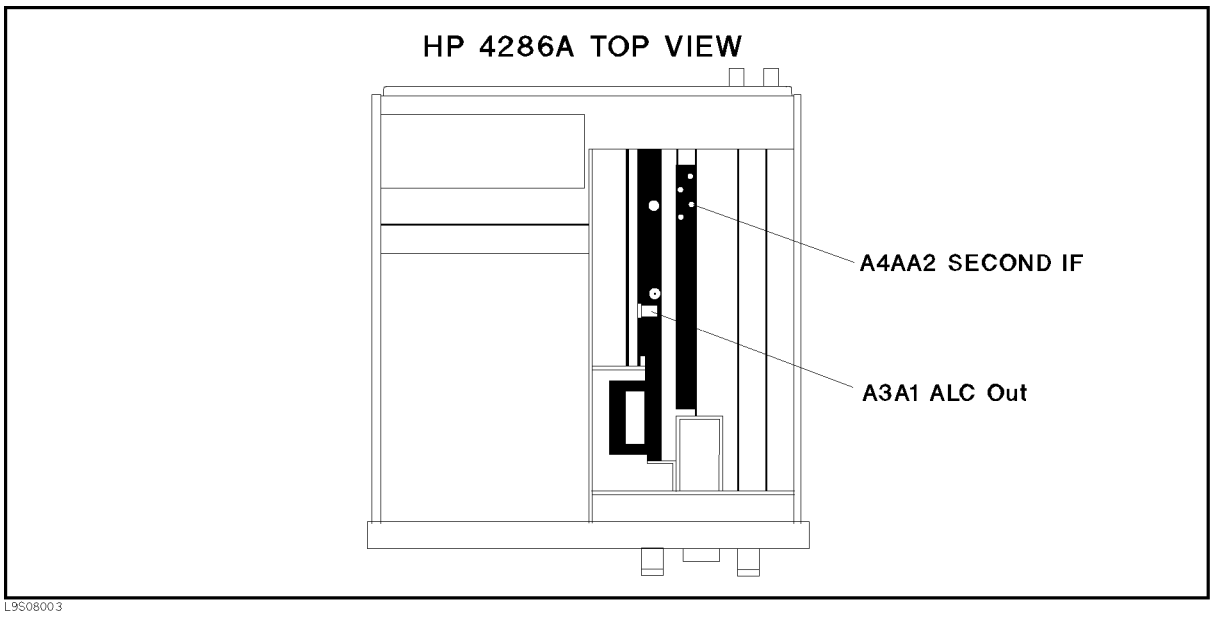

Figure 8-3. A6 GAIN Test Location

4. Turn the HP 4286A power on.
5. Press (System), SERVICE MENUS, TESTS, (2), (1), (x1) to access the A6 GAIN test. When "A6 GAIN" is displayed, press EXECUTE TEST.
6. Perform the test according to the displayed instructions.
   - If the test passes, reconnect the cables and replace the A4 First LO/Receiver RF.
   - If the test fails, replace the A6 receiver IF and reconnect the cables.

7. Press ⇧ once to access the V/I Normalizer test. When "A6 VI NORMALIZER" is displayed, press `EXECUTE TEST`.
8. Perform the test according to the displayed instructions.
   - If the test passes, continue with the next step.
   - If the test fails, replace the A6 receiver IF.
9. Press ⇧ once to access the FRONT ISOL'N test. When "FRONT ISOL'N" is displayed, press `EXECUTE TEST`.
10. Perform the test according to the displayed instructions.
    - If the test passes, the receiver group is probably operating correctly.
    - If the test fails, go to the *FRONT ISOL'N Test Failure Troubleshooting* procedure.

FRONT ISOL'N Test Failure Troubleshooting

In the FRONT ISOL'N test, the receiver gain is tested first. Then the isolation between the front S and R connectors is tested. Troubleshoot the analyzer as follows when this test fails:

- When "RECEIVER GAIN OUT OF SPEC" appears, confirm the connection between S and R connectors, and perform the test. If the test still fails, replace the A4 First Lo/Receiver RF.
- When "FRONT ISOL'N TEST FAILED" appears, check the connectors and semi-rigid cables connected to A3 and A4. Loose connectors and cracked cables can affect the isolation.

9

Test Head Troubleshooting

INTRODUCTION

This chapter provides procedures to isolate the faulty assembly in the test head.

Note

Use these procedures only if you have read Chapter 4 and you believe the problem is in the test head.

The troubleshoot procedures use the HP 4286A self-test function (external test). Remember that the self-test is done on the assumption that the source group and receiver group are operating correctly.

Allow the HP 4286A to warm up for at least 30 minutes before you perform any procedure in this chapter.

Figure 9-1 is a test head simplified block diagram. For more information about circuit operation, see Chapter 11.

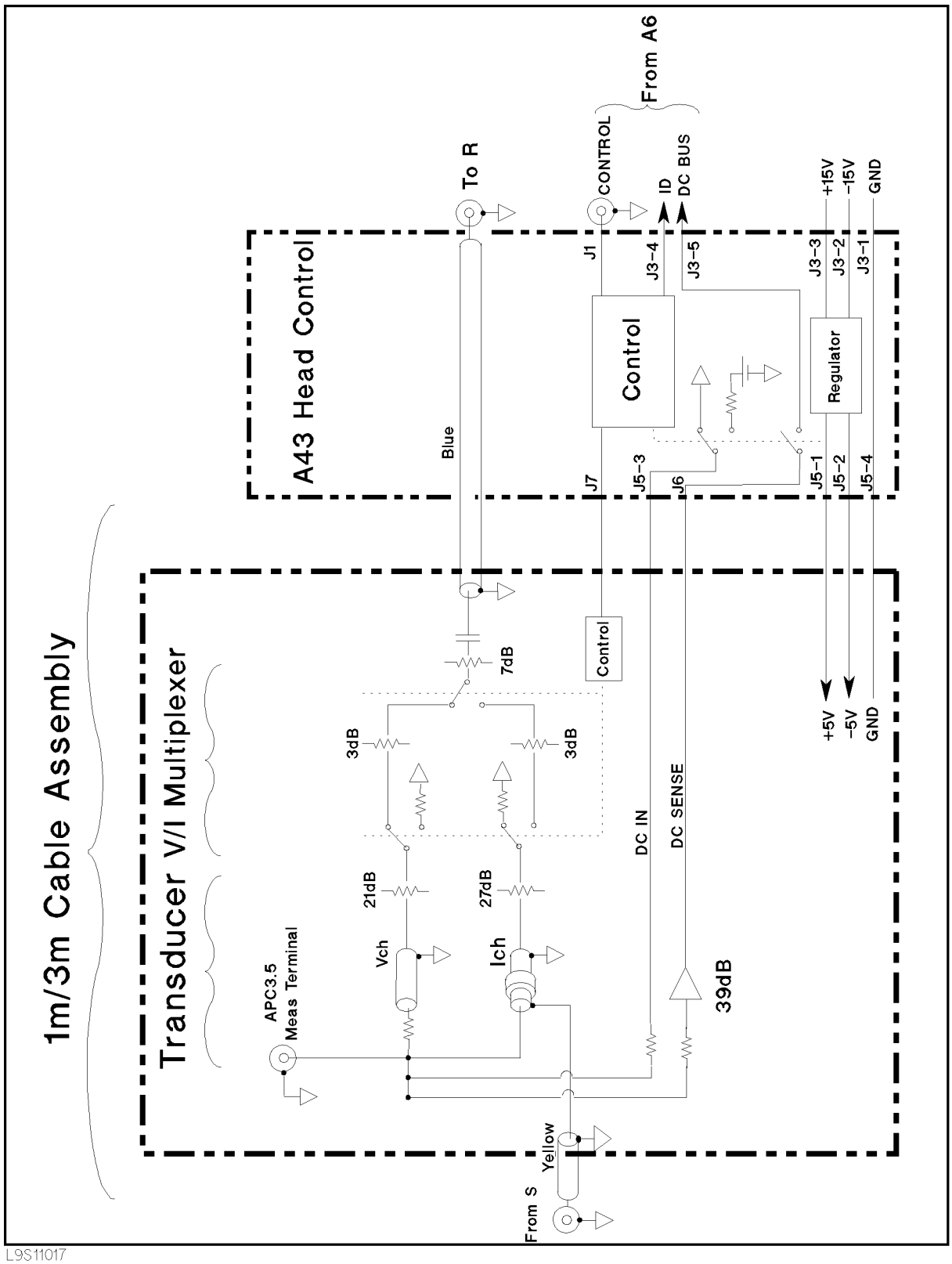

Figure 9-1. Test Head Block Diagram

TEST HEAD TROUBLESHOOTING

Performing the Test Head Diagnostic Test

Perform the TEST HEAD diagnostic test. If the test fails, the test head is faulty.

1. Turn the HP 4286A power on.
2. Press (SYSTEM), SERVICE MENU, TESTS, (2), (4), (x1) to access the TEST HEAD diagnostic test.
3. Press EXECUTE TEST to perform the test. The test procedure is as follows:

   a. Connect the HP 4286A S and R connectors with the N(m)-N(m) cable, and press CONT. The HP 4286A mainframe is calibrated for the test.

   b. Connect the test head to the mainframe, and connect the APC3.5(m)-APC7 adapter to the test head using the test fixture stand as shown in Figure 9-2.

   c. Connect the open termination of the APC7 calibration kit to the test head, and press CONT. The open measurement test is performed.

   d. In the same manner, perform the short and 50 Ω measurement tests with the short and 50 Ω terminations of the APC7 calibration kit, following the displayed instructions.

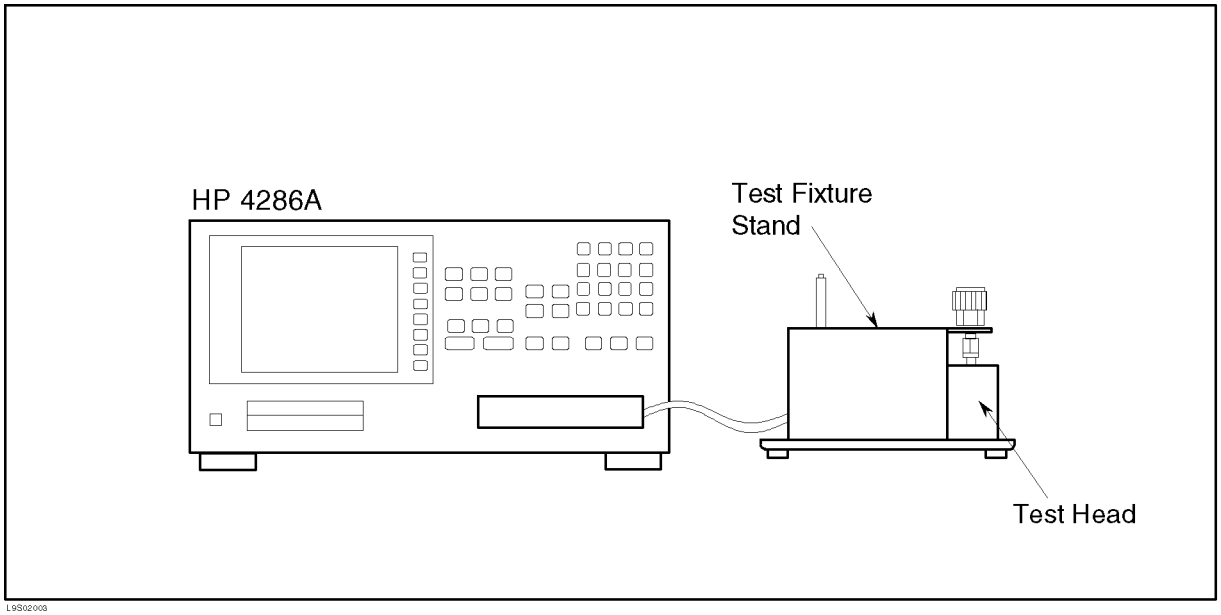

Figure 9-2. Test Head Diagnostic Test Setup

In the TEST HEAD diagnostic test, the signal voltages (the V-channel voltage, the I-channel voltage, and the voltage ratio of V-channel/I-channel) and the DC voltage across the DUT are tested.

If the signal voltage test fails, the test program is paused with the message "LIMIT: FAIL" at the end of each signal voltage test (and the `CONT` softkey appears).

If the DC voltage test fails, the test program is paused with the message "RDC LIMIT TEST FAIL" at the end of DC voltage test (and the `CONT` softkey appears) .

The test head consists of the two blocks : A43 head control block, and the Transducer-V/I Multiplexer block (the box with the APC3.5 measurement terminal). If you want to isolate the faulty block between these two blocks, use the following procedures.

When the Signal Voltage Test Fails

When the TEST HEAD diagnostic test is paused with the message "LIMIT: FAIL", use the following procedure.

1. Remove the eight screws which hold two N(m)-SMA(f) adapters.
2. Remove the top cover of the head control block to access the test points on A43.
3. Attach the two N(m)-SMA(f) adapters to the test head bottom cover by tightening the four screws, and connect the test head to the mainframe.
4. Disconnect the coaxial cable (black) from A43J7, and turn the HP 4286A on.
5. Check the output signal from A43J7 (the test head control signal for the V/I Multiplexer block) with an oscilloscope. See (a) of Figure 9-3.
   - If the result is good, the A43 is supplying the control signal correctly to the V/I Multiplexer block. The trouble is probably in the Transducer-V/I Multiplexer block.
   - If the result is bad, continue with the next step.
6. Turn the HP 4286A off, and reconnect the coaxial cable (black) to A43J7.
7. Remove the coaxial cable from A43J1, and turn the HP 4286A on.
8. Check the test head control signal from the mainframe by probing the coaxial cable center conductor. See (b) of Figure 9-3.
   - If the result is good, the trouble is probably in the A43 head control.
   - If the result is bad, check the coaxial cable that provides the control signal from the mainframe.

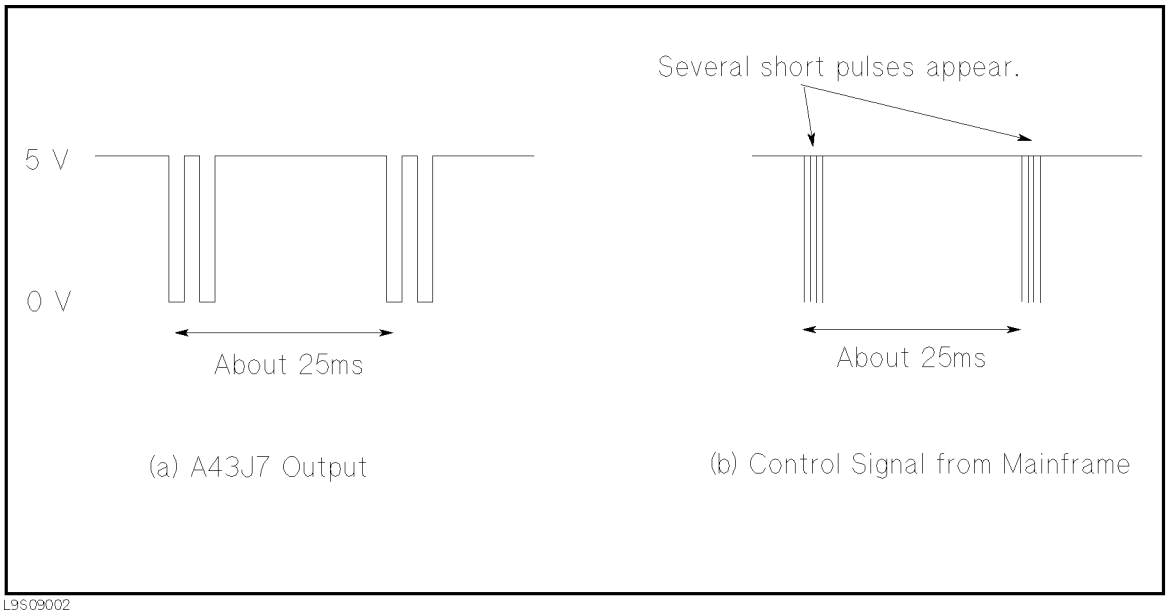

Figure 9-3. Test Head Control Signal Check

When the DC Voltage Test Fails

When the TEST HEAD diagnostic test is paused with the message "RDC LIMIT TEST FAIL", use the following procedure.

Check the A43 DC Voltage Source

1. Remove the eight screws which hold two N(m)-SMA(f) adapters.
2. Remove the top cover of the head control block to access the test points on A43.
3. Attach the two N(m)-SMA(f) adapters to the test head bottom cover by tightening the four screws, and connect the test head to the mainframe.
4. Connect the APC7 open termination to the measurement terminal.
5. Turn the HP 4286A on.
6. Press (Contact Check), `RDC MEAS on OFF` to turn on the DC resistance measurement function.
   The menu changes to `RDC MEAS ON off`.
7. Check the A43 DC voltage source output with an oscilloscope, probing the wire (orange) connected to A43J5 pin-3. See (a) of Figure 9-4.
   - If the result is good, continue with the step 10.
   - If the result is bad, continue with the step 8.
8. Turn the HP 4286A off, and disconnect the wire from A43J5.
9. Turn the HP 4286A on, and check the A43 DC voltage source output at A43J5 pin-3. See (b) of Figure 9-4.
   - If the result is good, the A43 DC source is probably not being supplied to the Transducer block due to trouble in the Transducer block.
   - If the result is bad, the DC voltage source circuit in the A43 head control is probably faulty.

Check the DC Voltage Measurement Value

10. Turn the HP 4286A off, and disconnect the coaxial cable (red) from A43J6
11. Turn the HP 4286A on, and check the output voltage from the coaxial cable (the DC voltage measurement result that comes from the Transducer block). See (c) of Figure 9-4.
    - If the result is good, continue with the next step.
    - If the result is bad, the DC voltage measurement circuit in the Transducer block is probably faulty.
12. Turn the HP 4286A off, and reconnect the coaxial cable to A43J6.
13. Turn the HP 4286A on, and check the output of the wire (green) connected to A43J3 pin-5. Normally, the result should be same as (c) of Figure 9-4.
    - If the result is good, check the wire to the A20 motherboard.
    - If the result is bad, the trouble is in the A43 head control.

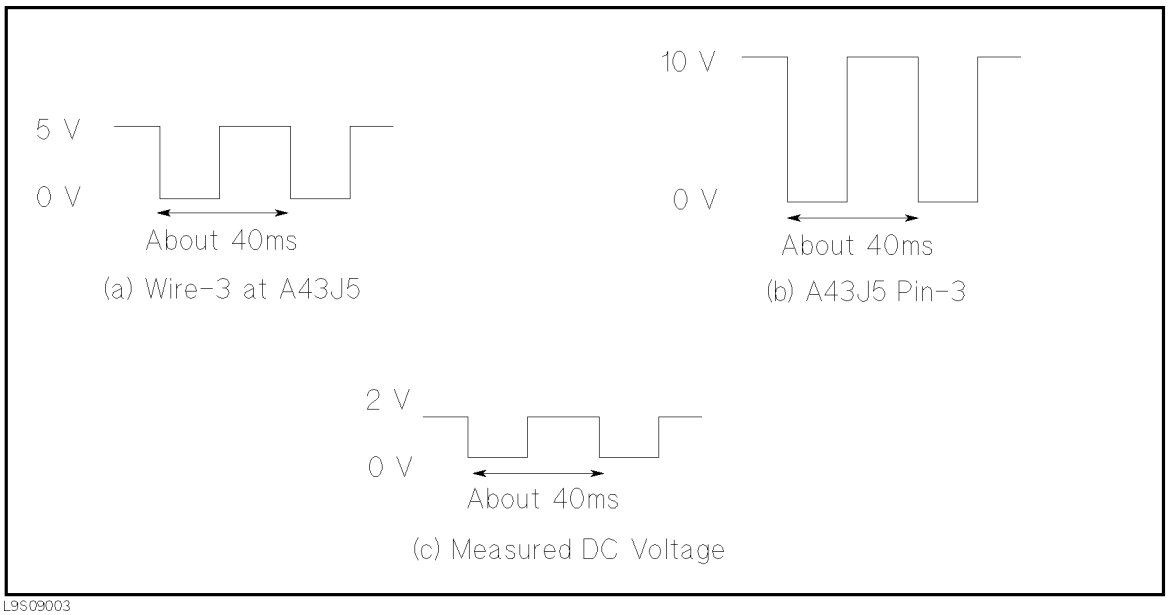

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Figure 9-4. DC Voltage Check (DUT: Open)

10

Service Key Menus

INTRODUCTION

The service key menus are used to test, verify, adjust, and troubleshoot the HP 4286A. They are also used to install and update the firmware in the HP 4286A.

The service key menus consist of several menus that are accessed through the service menu and the Bootloader menu as shown in Figure 10-1. The service menu is displayed by pressing (System), SERVICE MENU. The Bootloader menu is displayed by turning the HP 4286A power on while pressing (Trigger) and (Preset).

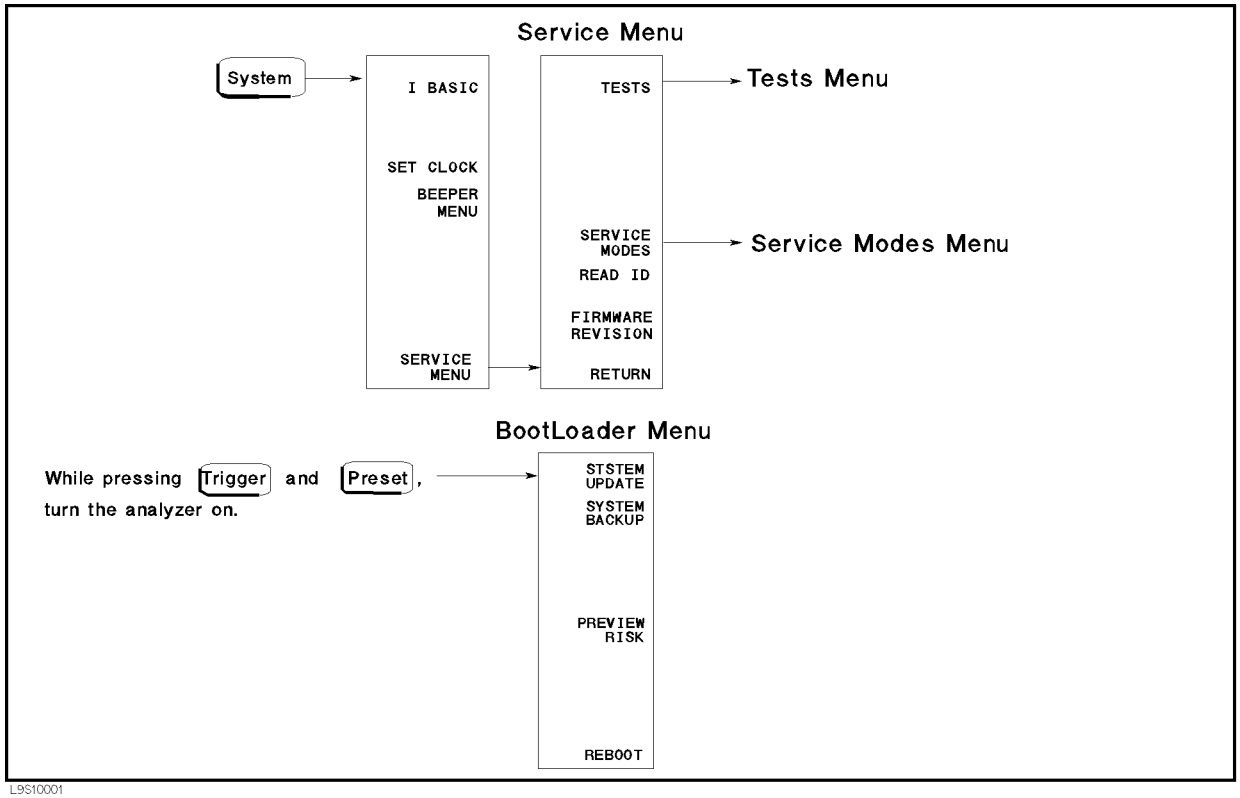


Figure 10-1. Service Key Menus

The service key menus allow you to perform the following functions:

- Select and execute a built-in diagnostic test. The HP 4286A has 37 built-in diagnostic tests. For detailed information, see the *Tests Menu* in this chapter.
- Control and monitor various circuits for troubleshooting. For detailed information, see the *Service Modes Menu* in this chapter.
- Display if the test head is connected or not.

- Display the firmware revision. See the *Service Menu* in this chapter.
- Install and update the firmware in the HP 4286A. For detailed information, see the *Bootloader Menu* in this chapter.

When applicable, the HP-IB mnemonic is written in parentheses following the softkey using the following symbol conventions:

{ }	A necessary appendage
<*numeric*>	A necessary numerical appendage
|	A delimiter for applicable appendages. For example, {OFF|ON|0,1|} means OFF, ON, 0, or 1.

For more about the HP-IB commands general information, see the *HP 4286A HP-IB Command Reference* .

SERVICE MENU

Figure 10-2 shows the service menu. This menu is used to display the tests menu, the service modes menu, and the firmware revision information. To display the service menu, press (System), SERVICE MENU. Each softkey in the service menu is described below.

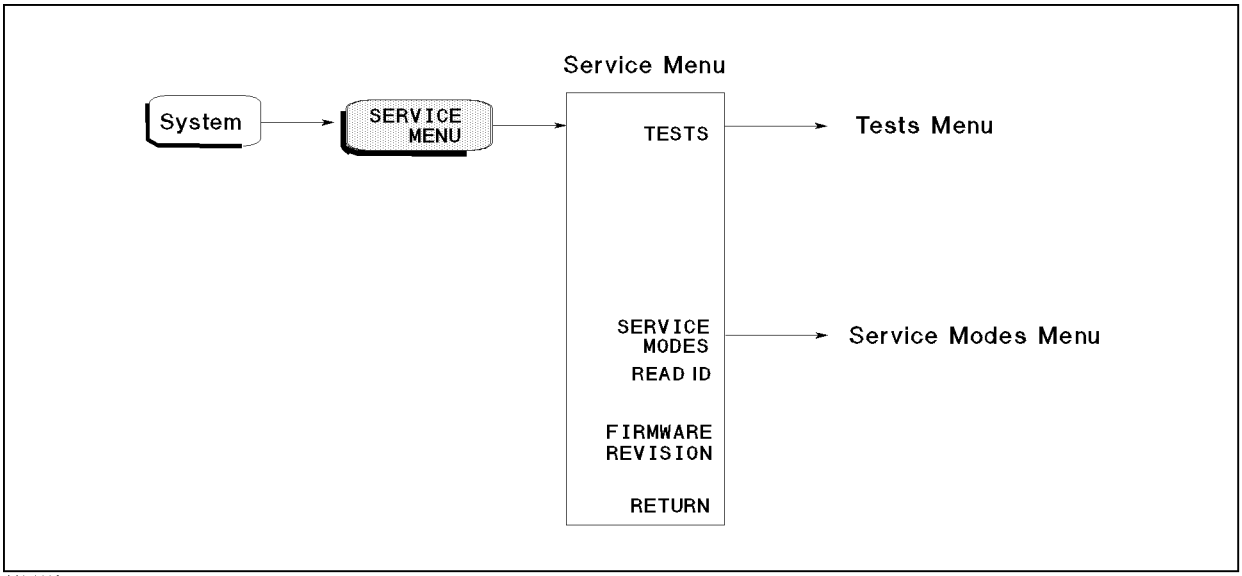


Figure 10-2. Service Menu

TESTS

Displays the tests menu. For more information about the tests menu, see the *Tests Menu* later in this chapter.

SERVICE MODES (:DIAG:SERV:MODE {ON|1})

Activates the service modes and displays the service modes menu. For more information about the service modes menu, see the *Service Modes Menu* later in this chapter.

READ ID

Displays if the test head is connected or not.

FIRMWARE REVISION (:DIAG:FREV?)

Displays the current firmware revision information. The number and implementation date appear in the active entry area of the display as shown below. Another way to display the firmware information is to cycle the HP 4286A power (off then on).

```
HP 4286A REVN.NN MON DD YEAR HH:MM:SS
```

where	N.NN:	Revision Number
	MON DD YEAR	Implementation Date (Month Day Year)
	HH:MM:SS	Implementation Time (Hour:Minute:Second)

TESTS MENU

Figure 10-3 shows the tests menu. The tests menu is used to select and execute one of the 37 built-in diagnostic tests. More information about the diagnostic tests is provided in the *Diagnostic Tests* later in this section. To display the tests menu, press (System), SERVICE MENU, and TESTS.

When entering the tests menu, internal test 0: ALL INT is selected as the default test. The test number, name, and status abbreviation is displayed in the active entry area of the display. See Figure 10-4. For the test status, see Figure 10-4.

The diagnostic tests are numbered from 0 to 36. To select a test, enter the desired test number using the numeric keypad, (↑), (↓) or HP-IB command (:DIAG:TEST <*numeric*>).

Each softkey in the tests menu is described below.

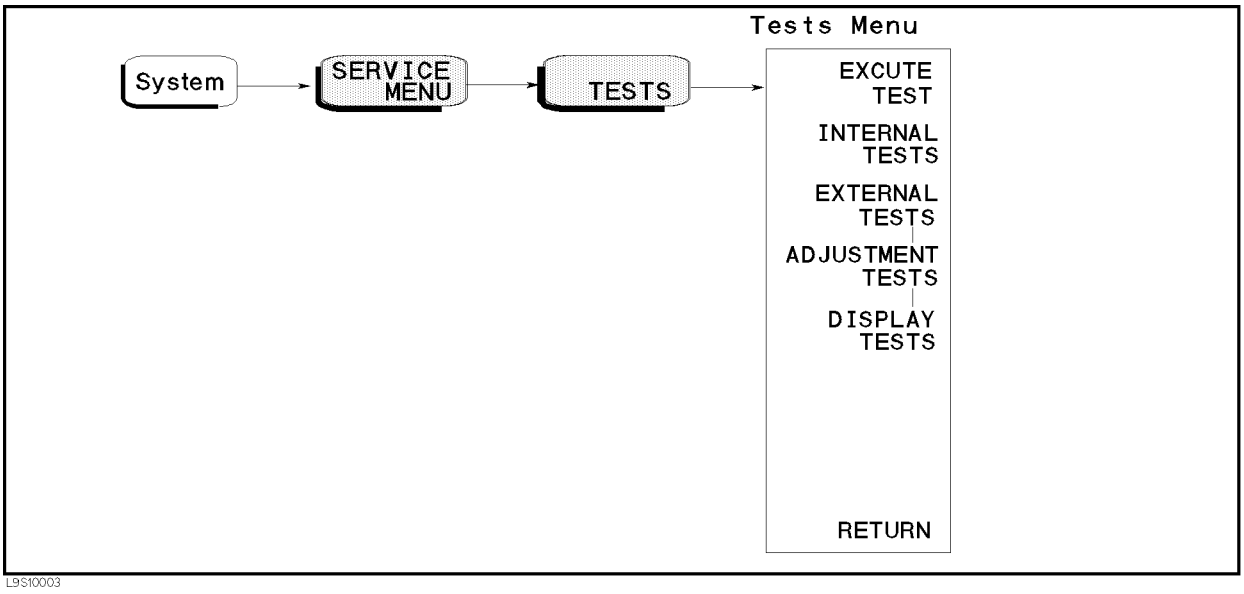


Figure 10-3. Tests Menu

EXECUTE TEST (:DIAG:TEST:EXEC)

Runs the selected test. When the executed test requires user interaction, CONT (:DIAG:TEST:CONT) and the instruction appear on the display. Follow the displayed instruction and press CONT to continue the test.

INTERNAL TESTS (:DIAG:TEST 0)

Selects the first internal test 0: ALL INT.

EXTERNAL TESTS (:DIAG:TEST 16)

Selects the first external test 16: FRONT PANEL DIAG.

ADJUSTMENT TESTS (:DIAG:TEST 26)

Selects the first adjustment test 26: HOLD STEP ADJ.

DISPLAY TESTS (:DIAG:TEST 32)

Selects the first display test 32: TEST PATTERN 1.

Note

After executing a test by pressing EXECUTE TEST, an annotation (Svc) is displayed to indicate any tests executed and the HP 4286A settings changed to the test settings. To return the HP 4286A to normal operation, cycle the HP 4286A power (off then on), or press (PRESET).

Note

While any test is being executed, do not change the HP 4286A setting using the front-panel keys, the HP-IB, or the I-BASIC program (Option 1C2 only). If the setting is changed during test execution, the test result and the HP 4286A operation are undefined.

Test Status

When selecting a test, the test status abbreviation is displayed as shown in Figure 10-4.

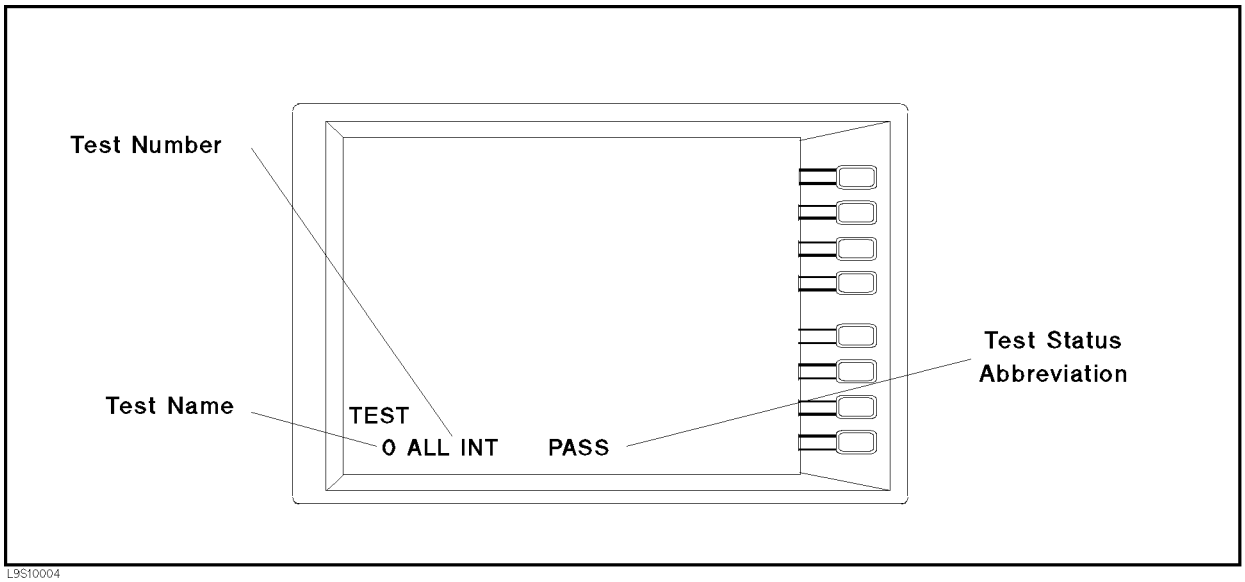


Figure 10-4. Test Status on the Display

To see the test status of the desired test, enter the desired test number using the numeric keypad, (↑), or (↓). Also, the three HP-IB commands listed below are available to get the test status using HP-IB.

`:DIAG:TEST:RES?` <*numeric*>	returns the test status. The <*numeric*> specifies the test number and is an integer from 0 to 36.
`*TST?`	executes internal test 0: ALL INT and returns the test result.
`:DIAG:INIT:RES?`	returns the power on self-test result.

A sample program using the command `:DIAG:TEST:RES?` is as shown below. This program displays the test status of internal test 1. See the *HP 4286A HP-IB Command Reference* for more information.

```
10    !
20    ASSIGN @Hp4286 TO 717 ! When iBASIC is used, replace "717" to "800."
30    !
40    OUTPUT @Hp4286;"DIAG:TEST:RES? 1"
50    ENTER @Hp4286;Test_status$
60    PRINT Test_status$
70    !
```

Sample Program Using `:DIAG:TEST:RES?`

Table 10-1 shows the test status abbreviation, its definition, and the HP-IB test status code.

Table 10-1. Test Status Terms

Status Abbreviation	Definition	HP-IB Code
PASS	Pass	"PASS"
FAIL	Fail	"FAIL"
-IP-	In progress	"BUSY"
-ND-	Not done	"NDON"
DONE	Done	"DONE"

The test status is stored in nonvolatile memory (battery backup memory). If the power to the nonvolatile memory is lost, the HP 4286A will set all test status abbreviations to "-ND-" (not done). If a test is aborted by pressing any key during its execution, the test status is undefined.

Diagnostic Tests

The HP 4286A has 37 built-in diagnostic tests. The HP 4286A performs the power on self-test every time the power on sequence occurs (when the HP 4286A is turned on). These tests are used to test, verify, adjust, and troubleshoot the HP 4286A.

The 37 built-in diagnostic tests are divided by function into three categories: internal tests, external tests, and adjustment tests. Each group is described below. Descriptions of the tests in each category are given in the *Test Descriptions* section. To access the first test in each category, the category softkey is available in the tests menu.

The power on self-test consists of internal tests 1 and 4 through 14. They are executed in the listed order. If any of the tests fail, that test displays a "`POWER ON TEST FAILED`" message at the end of the power on sequence. The first failed test indicates the most probable faulty assembly.

Internal Test	These tests are completely internal and self-evaluating. They do not require external connections or user interaction. The HP 4286A has 16 internal tests.
External Tests	These are additional self-evaluating tests. However, these tests require some user interaction (such as key entries). The HP 4286A has 10 external tests.
Adjustment Tests	These tests are used to adjust the HP 4286A. See the *Adjustments and Correction Constants* chapter. The HP 4286A has 6 adjustment tests.
Display Tests	These tests are used to adjust and check for proper operation of the display circuits. See the *Adjustments and Correction Constants* chapter. The HP 4286A has 5 display tests.

Test Descriptions

This section describes all 68 diagnostic tests.

INTERNAL TESTS

This group of tests run without external connections or operator interaction. All return a "PASS" or "FAIL" indication on the display. Except as noted, all are run during the power on self-test and when (Preset) pressed.

0: ALL INT

Runs only when selected. It consists of internal tests 1 and 4 through 14. If any of these tests fail, this test displays the "FAIL" status indication. Use (⇧) or (⇩) to scroll through the tests to see which test failed. If all pass, the test displays the "PASS" status indication. Each test in the subset retains its own test status.

1: A1 CPU

Verifies the following circuit blocks on the A1 CPU:

- Digital Signal Processor (DSP)
- System Timer
- Real Time Clock
- Front Key Controller
- Flexible Disk Drive Controller
- HP-IB Controller
- EEPROM

2: A1 VOLATILE MEMORY

Runs only when selected. It verifies the A1 volatile memories:

CPU internal SRAM
DSP SRAM
Dual Port SRAM
Backup SRAM

At the end of the test, the HP 4286A is set to the power-on default state because the data in the tested memories is destroyed. During this test, a test pattern is written into the memories and then the pattern is read back and checked.

If the test fails, the test displays an error message for a few seconds and then sets the HP 4286A to the default state. The error message indicates the faulty memory.

3: A51 GSP

Runs only when selected. It verifies the following circuit blocks on the A51 GSP:

GSP Chip
DRAM
VRAM

At the end of this test, the HP 4286A is set to the power-on default state because the data in the tested memories is destroyed. During this test, a test pattern is written into the memories and then the pattern is read back and checked.

After the HP 4286A is set to the power-on default state, press (SYSTEM), SERVICE MENU, TESTS, (3), (x1) again. Then the test result is displayed at the lower part of the CRT.

4: A2 POST REGULATOR

Verifies all A2 post regulator output voltages:

+5 V(AUX), +15 V(AUX)
−15 V, −12.6 V, −5 V, +5 V, +5.3 V, +8.5 V, +15 V,
+22 V, +65 V, FAN POWER, GND

This test measures the A2 output voltages at DC bus nodes 1 through 12, and 26. It checks that each measured value is within limits.

5: A6 A/D CONVERTER

Verifies the following circuit blocks on the A6 Receiver IF:

A/D Converter
Gain Y
Gain Z
Range R

This test measures the A/D converter's reference voltage (VREF) at DC bus node 25 through the gain Y, the gain Z, and the range R. These circuits are set to several settings in the test. For each setting, this test checks that the measured value is within limits.

6: A5 REFERENCE OSC

Verifies the reference oscillator in the A5 synthesizer. This test measures the VCO tuning voltage at DC bus node 22 and the frequency (2.5 MHz) at frequency bus node 6. It then checks that each measured value is within limits.

7: A5 FRACTIONAL N OSC

Verifies the fractional N oscillator in the A5 synthesizer. This sets the oscillator frequency to several frequencies over the entire range. For each setting, this test measures the VCO tuning voltage at DC bus node 20 and the frequency at frequency bus node 4. It then checks that each measured value is within limits.

8: A4A1 1ST LO OSC

Verifies the 1st LO oscillator in the A4A1 1st LO. This test sets the oscillator frequency to several frequencies over the entire range. For each frequency, the test measures the VCO tuning voltage at DC bus node 18 and checks that each measured value is within limits.

9: A3A2 2ND LO OSC

Verifies the 2nd LO oscillator in the A3A2 2nd LO. This test measures the VCO tuning voltage at DC bus node 14 and checks that the measured value is within limits.

10: A3A1 DIVIDER

Verifies the divider circuit in the A3A1 Source Vernier. This test measures the frequency (40 kHz) at frequency bus node 2 and checks that the measured value is within limits.

11: A6 3RD LO OSC

Verifies the 3rd LO oscillator on the A6 receiver IF. This test measures the VCXO tuning voltage at DC bus node 23 and the frequency (40 kHz) at frequency bus node 6. It then checks that each measured value is within limits.

12: A3A1 SOURCE OSC

Verifies the source oscillator in the A3A1 Source Vernier. This test measures the VCXO tuning voltage at DC bus node 13 and the frequency (40 kHz) at frequency bus node 1. It then checks that each measured value is within limits.

13: A6 SEQUENCER

Verifies the A/D sequencer circuit in the A6 receiver IF. This test measures the frequency (80 kHz) of the A/D sequence output at frequency bus node 7 and checks that the measured value is within limits.

14: SOURCE LEVEL

Verifies the source circuit. This test measures the A3A3 output at DC bus node 15 in A3A1. It then checks that each measured value is within limits.

15: A33 MEMORY DISK

Verifies the backup SRAM on the A33 handler interface board . At the end of this test, the HP 4286A is set to the power-on default state because the data in the tested memories is destroyed. During this test, a test pattern is written into the memories and then the pattern is read back and checked.

EXTERNAL TESTS

This group of tests require either external equipment and connections or operator interaction to run. These tests are used in the *Troubleshooting* chapter.

16: FRONT PANEL DIAG.

Checks all front-panel keys on the A30 keyboard. The abbreviated name is displayed when pressing one of the keys.

17: DSK DR FAULT ISOL'N

Checks the FDD (Flexible Disk Drive). When this test is started, a bit pattern is written to the flexible disk. Then the pattern is read back and checked. This write pattern check is repeated from the low to high addresses.

Note After this test is performed, the data stored on the floppy disk is lost.

18: SOURCE FLATTNESS

Checks that the source flatness is within limits. As a result, A3A1, A3A2 and A3A3 are verified.

The HP 4286A mainframe "S" and "R" connectors are connected, and the "S" output level is measured at the "R" input.

19: OUTPUT ATTENUATOR

Checks that the A7 attenuation accuracy is within limits. As a result, A7 is verified.

The HP 4286A mainframe "S" and "R" connectors are connected, and the "S" output level is measured at the "R" input.

20: RECEIVER GAIN

Checks that the receiver circuit gain is within limits. As a result, A4A2 and A6 are verified.

The HP 4286A mainframe "S" and "R" connectors are connected, and the "R" input gain is tested using the "S" output.

21: A6 GAIN

Checks that the A6 gain is with in limits. As are result, A6 is verified.

The A3A1 21.42 MHz output is directly applied to the A6 input.

22: A6 V/I NORMALIZER

Checks that the A6 V/I normalizer (GAIN X, Y, and Z) gain change is within limits. As a result, A6 is verified.

The HP 4286A mainframe "S" and "R" connectors are connected, and the "R" input gain change is tested using the "S" output.

23: FRONT ISOL'N

Checks that the HP 4286A mainframe front isolation is enough.

The HP 4286A mainframe "S" and "R" connectors are connected, and the "S" output level is measured at the "R" input. Then "S" and "R" connectors are terminated with 50 Ω terminatoins, and the "R" measurement result is compared with the previous measurement result.

24: TEST HEAD

Checks that the HP 4286A test head characteristics are correct. As a result, the test head is verified.

The HP 4286A mainframe "S" and "R" connectors are connected, and the HP 4286A mainframe is calibrated. Then the test head characteristics are verified while connecting the 0 S, 0 Ω and 50 Ω terminations of the APC7 calibration kit. The test result is displayed at the lower part of the CRT after all of three termination tests are completed.

25: A33 HANDLER INTERFACE

Checks the handler interface function. When performing this test, the toggle switch and bit switchs on the A33 handler interface must be factory default setting shown in the HP 4286A top shield cover.

The handler simulator (PN 04278-65001) is connected to the rear panel handler interface connector with the cable (PN 04278-61635). If all the LEDs (except the LEDs that are not used. See Table 10-2.) on the handler simulator simultaneously blink several times, the handler interface function is correct.

Table 10-2. Handler Interface Function Test

Handler Simulator LED No.	HP 4286A Signal To Be Tested
LED1 (BIN1) to LED9 (BIN9)	/BIN1 to /BIN9
LED10 (OUT OF BIN)	/OUT OF BIN
LED11 (BIN10)	/AUX BIN
LED12 (PHI)	/PHI
LED13 (PLO)	/PLO
LED14 (SREJ)	/SREJ
LED15 (OVFL)	/FAIL
LED16 (UNDFL)	(Not used)
LED17 (UNBAL)	/NO CONTACT
LED18 (EOM)	/EOM
LED19 (EXT TRG)	(Not used)[1]
LED20 (INDEX)	/INDEX
LED21 (ALARM)	/ALARM
LED22 (CH1) to LED25 (CH.4)	(Not used)[1]

1 Ignore the blink of this LED.

ADJUSTMENT TESTS

This group of tests is used when adjusting the HP 4286A. These tests make the adjustment procedure easier. For more detailed operating information, see Chapter 3.

26: HOLD STEP ADJ

Used when the *Hold Step Adjustment* on the A6 receiver IF is performed.

27: BPF ADJ

Used when the *Band Pass Filter Adjustment* on the A6 receiver IF is performed.

28: 3RD VCXO LEVEL ADJ

Used when the *Third Local VCXO Adjustment* on the A6 receiver IF is performed.

29: 2ND LO PLL LOCK ADJ

Used when the *Second Local PLL Lock Adjustment* on the A3A2 2nd LO is performed.

30: SOURCE VCXO LEVEL ADJ

Used when the *Source VCXO Adjustment* on the A3A1 level vernier is performed.

31: SOURCE MIXER LEAK ADJ

Used when the *Source Mixer Local Leakage Adjustment* on the A3A2 2nd LO is performed.

DISPLAY TESTS

These tests are test patterns that are used in the factory for display adjustments, diagnostics, and troubleshooting. Test patterns are executed by entering the test number (32 through 36), then pressing `EXECUTE TEST`, `CONTINUE`. The test pattern is displayed and the softkey labels are blanked. To exit the test pattern and return to the softkey labels, press softkey 8 (on the bottom). The following is a description of the test patterns.

Note

Do NOT press any keys except softkey 8 (on the bottom) while the test pattern is being executed. If you do, you CANNOT quit the test pattern (that is, you can quit the test pattern only when the HP 4286A is turned OFF).

32: TEST PATTERN 1

All Green. This pattern is used to adjust vertical position and size. See the *Display Adjustment* in the *Adjustments and Correction Constants* chapter for more information. Also this test pattern is convenient for adjusting the CRT Intensity from the front panel.

33: TEST PATTERN 2

Crosshatch. This pattern is used to adjust vertical synchronization, horizontal position, vertical linearity, and focus. See the *Display Adjustment* in the *Adjustments and Correction Constants* chapter for more information.

34: TEST PATTERN 3

Inverse Crosshatch. This test pattern is used for the same purpose as TEST PATTERN 2. (Normally, the vertical lines don't appear.)

35: TEST PATTERN 4

Character Set. The character set is provided to conveniently show the user all the different types and sizes of characters available. Three sets of characters are drawn in each of the three available character sizes. All 125 characters of each size are displayed. Characters 0 and 3 are not displayed and others are non-displayable control characters (such as carriage return and line feed).

36: TEST PATTERN 5

Bandwidth Pattern. This pattern provides a quick visual verification of the display bandwidth. It consists of multiple alternating green and black vertical stripes. Each stripe should be clearly visible. A limited bandwidth will appear to smear these lines together.

SERVICE MODES MENU

Figure 10-5 shows the service modes menu. The service modes menu leads to one of the menus used to control the HP 4286A service modes. For the HP 4286A's service modes, see the *Service Modes* . To display the service modes menu, press (System), SERVICE MENU, and SERVICE MODES. Each softkey in the service modes menu is described below.

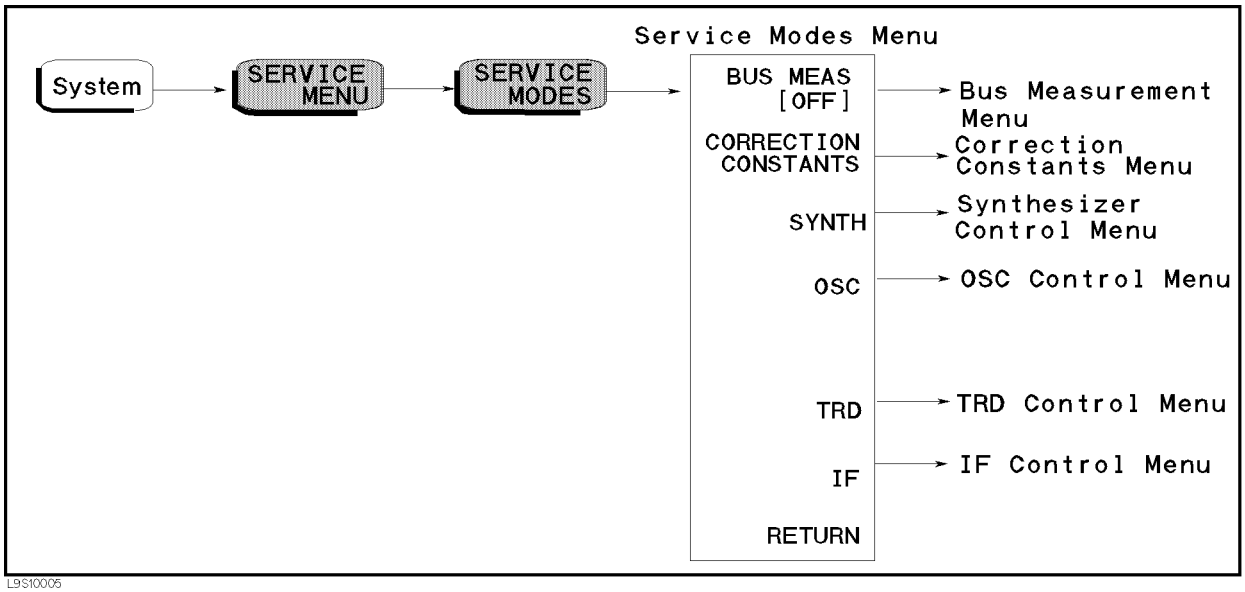


Figure 10-5. Service Modes Menu

BUS MEAS [OFF]

Displays the Bus Measurement Menu. See the *Bus Measurement Menu* in this chapter.

CORRECTION CONSTANTS

Displays the Correction Constant Menu. See the *Correction Constant Menu* in this chapter.

SYNTH

Displays the Synthesizer Control Menu. See the *Synthesizer Control Menu* in this chapter.

OSC

Displays the OSC Control Menu. See the *OSC Control Menu* in this chapter.

TRD

Displays the Transducer Control Menu. See the *Transducer Control Menu* in this chapter.

IF

Displays the IF Control Menu. See the *IF Control Menu* in this chapter.

Service Modes

The HP 4286A has various service modes. These service modes are powerful tools to test, verify, adjust, and troubleshoot the HP 4286A. The service modes are divided by function into the six groups listed below:

Bus Measurement	measures and displays the signal voltage or frequency at the selected bus node of the HP 4286A. This service mode allows you to check the circuit operation by monitoring the circuit signal without accessing the inside ofthe HP 4286A.
Correction Constants On/Off	allows you to turn one (or more) of the corrections on/off.
Synthesizer Control	allows you to control the internal circuit settings in the A5 synthesizer.
OSC Control	allows you to control the internal circuit settings in the A3A1 Source Vernier.
Transducer Control	allows you to control the internal circuit settings in the test head.
IF Control	allows you to control the internal circuit settings in the A6 receiver IF.

Note

After pressing SERVICE MODES, an annotation (Svc) is displayed to indicate that the service modes are activated. The settings made in the service modes are kept until the HP 4286A is turned off or [PRESET] is pressed.

BUS MEASUREMENT MENU

Figure 10-6 shows the bus measurement menu. This menu is used to control the bus measurements. For more information about the bus measurements, see the *Bus Measurement*. For the bus measurement procedure, see the *Bus Measurement Procedure* .

To display the bus measurement menu, press (System), SERVICE MENU, SERVICE MODES, and BUS MEAS [ ]. Each softkey in the bus measurement menu is described below.

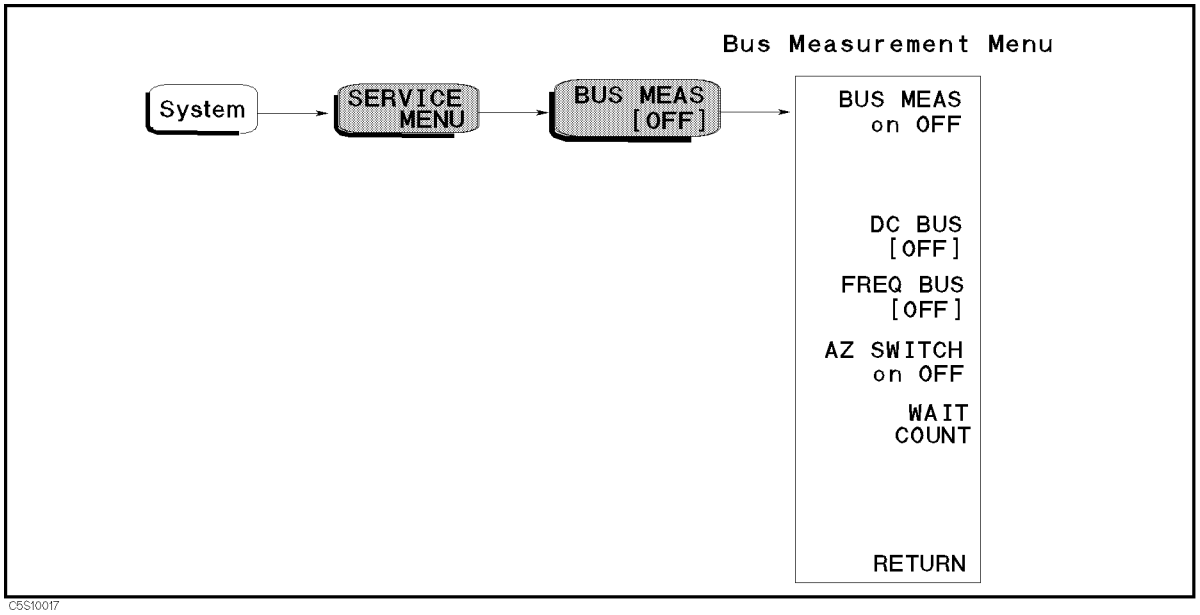


Figure 10-6. Bus Measurement Menu

BUS MEAS on OFF (:DIAG:SERV:BUS:STAT {ON|OFF})

Toggles the bus measurement on and off. After pressing this softkey, the menu changes to BUS MEAS ON off and the measured value of the bus measurement is displayed.

DC BUS [OFF] (:DIAG:SERV:BUS:DC <*numeric*>)

Allows you to select one of the DC bus nodes. The DC bus nodes are numbered from 0 to 29. To select the desired DC bus node, press this softkey and then enter the node number by using the numeric keypad, (↑), or (↓). The node number and name are displayed in the active entry area of the display and the node abbreviation is displayed in the brackets of the menu.

FREQ BUS [OFF] (:DIAG:SERV:BUS:FREQ <*numeric*>)

Allows you to select one of the frequency bus nodes. The frequency bus nodes are numbered from 0 to 7. To select the desired frequency bus node, press this softkey and then enter the frequency node number by using the numeric keypad, (↑), or (↓). The node number and name are displayed in the active entry area of the display and the node abbreviation is displayed in the brackets of the menu.

`AZ SWITCH on OFF` (:DIAG:SERV:BUS:AZER {OFF|ON|0|1})

Toggles the auto zero switch on and off.

`WAIT COUNT` (:DIAG:SERV:BUS:WAIT <*numeric*>)

Sets the wait count to specify the wait time in the DC bus measurement. The wait count is an integer from 2 to 32767. When the wait count is N, the HP 4286A waits N * 12.5 μsec before each DC bus measurement.

Bus Measurement

In this service mode, the HP 4286A measures and displays the signal voltage or frequency at the selected bus node. This service mode allows you to check the circuit operation by monitoring the circuit signal without accessing the inside of the HP 4286A.

The HP 4286A has 36 bus nodes for this service mode. Of these, 29 bus nodes are for DC voltage measurement. These nodes are connected to the A/D converter in the A6 receiver IF through the DC Bus, a single multiplexer line with twenty-nine channels. The other 7 bus nodes are for frequency measurement. These nodes are connected to the frequency bus timer in the A1 CPU through the frequency bus, a single multiplexer line with 7 channel.

Each of the DC bus nodes and the frequency bus nodes is described in the *DC Bus Nodes* and *Frequency Bus Nodes* in this section.

Bus Measurement Procedure

Use this procedure to perform the bus measurement.

1. Press (Preset) to initialize the HP 4286A.
2. Set the HP 4286A controls to the settings that you desire to observe in the bus measurement.
3. Press (System), `SERVICE MENU`, `SERVICE MODES`, `BUS MEAS` to display the bus measurement menu.
4. Select the desired bus node as follows:
   - If a DC bus measurement is desired, press `DC BUS [OFF]`. Then enter a node number between 1 and 29.
   - If a frequency bus measurement is desired, press `FREQ BUS [OFF]`. Then enter a node number between 1 and 7.
5. Press `BUS MEAS on OFF` to activate the bus measurement. The menu changes to `BUS MEAS ON off`. The DC bus measurement value is displayed in the "R :" field, and the frequency bus measurement value is displayed in the "X :" field. See the *Bus Measurement Values* section.
6. Observe the bus measurement value.
7. Press (Preset) to exit the bus measurement.

To change the bus node to another node, repeat the steps above.

It is impossible to monitor both the DC bus and the frequency bus simultaneously. When you want to change the HP 4286A from the DC bus measurement mode to the frequency bus measurement mode, perform the following procedure.

1. Press `DC BUS` and select zero (off).
2. Press `FREQ BUS` and select the desired frequency bus measurement menu.
3. Turn off and on `BUS MEAS on OFF`.

Bus Measurement Values

The bus measurement value is displayed with a unit "U."

- The DC bus measurement's "1 U" is equivalent to "1 V." The displayed value in the DC bus measurement does not corresponding to the measured voltage because the voltage detected at the DC bus node is scaled appropriately and measured. The scaling factor depends on each DC node. For example, the scaling factor at the DC bus node 1 of +5 V (AUX) is approximately 0.405. Therefore the displayed value is nominally 2.025 U (5 U x 0.405). A typical value for each DC bus node measurement is provided in the *DC Bus Node Descriptions*.
- The frequency bus measurement's "1 U" is equivalent to "1 MHz." For example, a measured value of 1 kHz is displayed as 1 mU. A typical value for each frequency bus measurement is provided in the *Frequency Bus Node Descriptions*.

DC Bus Node Descriptions

The following paragraphs describe the 26 DC bus nodes. They are listed in numerical order.

0: OFF

The DC bus is off. This is the default setting.

1: + 5 V (AUX) (2.025 U)

This node is located on the A2 post-regulator and detects the voltage of the +5 V (AUX) power supplied to the A2 post-regulator. The typical monitor value is +2.025 U (±10%).

2: −15 V (−1.92 U)

This node is located on the A2 post-regulator and detects the voltage of the +5 V (AUX) power supplied to the analog boards. The typical monitor value is -1.92 U (±10%).

3: −12.6 V (−2.124 U)

This node is located on the A2 post-regulator and detects the voltage of the −12.6 V power. The typical monitor value is -2.124 U (±10%).

4: −5 V (−2.025 U)

This node is located on the A2 post-regulator and detects the voltage of the −5 V power supplied to the analog boards. The typical monitor value is -2.025 U (±10%).

5: + 5 V (2.025 U)

This node is located on the A2 post-regulator and detects the voltage of the +5 V power supplied to the analog boards. The typical monitor value is +2.025 U (±10%).

6: + 5.3 V (2.1465 U)

This node is located on the A2 post-regulator and detects the voltage of the +5.3 V power supplied to the A3A3 source. The typical monitor value is +2.1465 U (±10%).

7: + 8.5 V (1.8955 U)

This node is located on the A2 post-regulator and detects the voltage of the +8.5 V power supplied to the A3A3 source. The typical monitor value is +1.8955 U (±10%).

8: +15 V (AUX) (1.92 U)

This node is located on the A2 post-regulator and detects the voltage of the +15 V (AUX) power. The typical monitor value is +1.8955 U (±5%).

9: +15 V (1.92 U)

This node is located on the A2 post-regulator and detects the voltage of the +15 V power supplied to the analog boards. The typical monitor value is +1.92 U (±10%).

10: +22 V (2.002 U)

This node is located on the A2 post-regulator and detects the voltage of the +22 V power. The typical monitor value is +2.002 U (±10%).

11: FAN POWER

This node is located on the A2 post-regulator and detects the voltage of the FAN POWER (nominal 24 V) supplied to the fan on the rear panel.

12: +65 V (2.0605 U)

This node is located on the A2 post-regulator and detects the voltage of the +65 V power supplied to the A52 DC-DC converter. The typical monitor value is +2.0605 U (±10%).

13: SRC VTUNE (Source Oscillator VCO Tuning Voltage)

This node is located in the source oscillator on the A3A1 Source Vernier and detects the 85.68 MHz VCO tuning voltage. The typical monitor value is within +0.1 U to +3.0 U.

14: 2ND LO VTUNE (Second Local Oscillator VCO Tuning Voltage)

This node is located in the second local oscillator on the A3A2 2nd LO and detects the 1.04 GHz VCO tuning voltage. The typical monitor value is within -130 mU to +130 mU.

15: DET OUT (Detector Output)

This node is located in the level detector circuit on the A3A1 Source Vernier and detects the level detector voltage that loops back from A3A3 source.

When the HP 4286A OSC level setting is 0.5 V, the typical monitor value is within -0.8 U to -0.2 U at 1 MHz, and -3.0 U to -0.5 U at 1 GHz.

16: SRC LO LEVEL

This node is located in the source oscillator circuit on the A3A1 Source Vernier and detects the source VCXO output voltage.

17: DAC OUT (Level DAC Output Voltage)

This node is located in the level vernier circuit on the A3A1 Source Vernier and detects the level DAC output voltage.

When the HP 4286A OSC level setting is 0.5 V, the typical monitor value is within +0.1 U to +0.8 U at 1 MHz, and +0.2 U to +1.6 U at 1 GHz.

18: 1ST LO VTUNE (First Local Oscillator VCO Turning Voltage)

This node is located in the 1st local oscillator on the A4A1 1st LO and detects the 2.05958 GHz to 3.05858 GHz VCO tuning voltage. The typical monitor value is within -2.3 U to -1.2 U at 1 MHz, and -1.4 U to +0.6 U at 1 GHz.

19: (Not Available)

20: FN VTUNE (Fractional N Oscillator VCO Turning Voltage)

This node is located in the fractional N oscillator on the A5 synthesizer and detects the 31.25 MHz to 62.5 MHz VCO tuning voltage. The typical monitor value is within -2.3 U to -0.5 U at 1 MHz, and -0.3 U to +1.2 U at 1 GHz.

21: FN INTEG OUT (Fractional N Oscillator Integrator Output Voltage)

This node is located in the fractional N oscillator on the A5 synthesizer and detects the integrator output voltage. The typical monitor value is within -3.0 U to -2.0 U at 1 MHz, and -0.5 U to +1.5 U at 1 GHz.

22: REF VTUNE (Reference Oscillator VCO Tuning Voltage)

This node is located in the reference oscillator on the A5 synthesizer and detects the 40 MHz VCXO tuning voltage. The typical monitor value is within 0 U to +3.0 U.

23: 3RD LO VTUNE (Third Local Oscillator VCO Tuning Voltage)

This node is located in the third local oscillator on the A6 receiver IF and detects the 85.6 MHz VCXO tuning voltage. The typical monitor value is within +0.1 U to +3.0 U.

24: 3RD LO LEVEL

This node is located in the A6 receiver IF and detects the third local oscillator signal level.

25: AD VREF (A/D Converter Voltage Reference)

This node is located in the A6 receiver IF and detects the reference voltage of the A/D converter. The typical monitor value at preset condition is within +0.16 U to +0.24 U.

26: RDC VOLTAGE

This node detects the DC voltage across the DUT.

When the OPEN / SHORT / 50 Ω is connected to the test head, the typical monitor value is +1.8 U to +2.6 U / -0.2 U to +0.2 U / +1.0 U to +1.4 U, respectively.

27: (Not Available)

28: (Not Available)

29: GND

This node is located on the A2 post-regulator and detects the ground voltage. The typical monitor value is within -0.1 U to 0.1 U.

Frequency Bus Node Descriptions

The following paragraphs describe the 6 frequency bus nodes. They are listed in numerical order.

0: OFF

The frequency bus is off. This is the default setting.

1: SOURCE OSC (Source Oscillator)

This node is located in the source oscillator on the A3A1 Source Vernier and measures the loop back frequency of 40 kHz from the 85.68 MHz VCO. The typical monitor value is within +39.992 mU to +40.008 mU.

2: DIVIDER OUT (Divider Output)

This node is located in the divider on the A3A1 Source Vernier and measures the 1/200 divider output frequency 40 kHz. The typical monitor value is within +39.992 mU to +40.008 mU.

3: (Not Available)

4: FN OSC (Fractional N Oscillator)

This node is located in the fractional N oscillator on the A5 synthesizer and measures the fractional N oscillator frequency through the 1/16 divider. The typical monitor value is within 2.0113 U ± 0.01 U at 1 MHz, and 2.9868 U ± 0.01 U at 1 GHz.

5: REF OSC (Reference Oscillator)

This node is located in the INT REF output circuit on the A5 synthesizer and measures the INT REF output frequency 10 MHz through the 1/4 divider. The typical monitor value is within +2.4996 U to +2.5004 U.

6: 3RD LO OSC (Third Local Oscillator)

This node is located in the third local oscillator on the A6 receiver IF and measures the loop back frequency of 40 kHz from the 85.6 MHz/85.68 MHz VCO. The typical monitor value is within +39.992 mU to +40.008 mU.

7: SAMPLE HOLD

This node is located in the sequencer on the A6 receiver IF and measures the 80 kHz sampling signal in the sequencer.

The typical monitor value is within +79.984 mU to +80.016 mU.

CORRECTION CONSTANTS MENU

Figure 10-7 shows the correction constants menu. This menu allows you to turn off the corrections. When the corrections are turned off, the HP 4286A displays the raw measured data. You can check the raw characteristics of the source circuit. For the corrections, see the *Correction Constants*.

To display the menu, press (System), SERVICE MENU, SERVICE MODES, and CORRECTION CONSTANTS. Each softkey in the correction constants menu is described below.

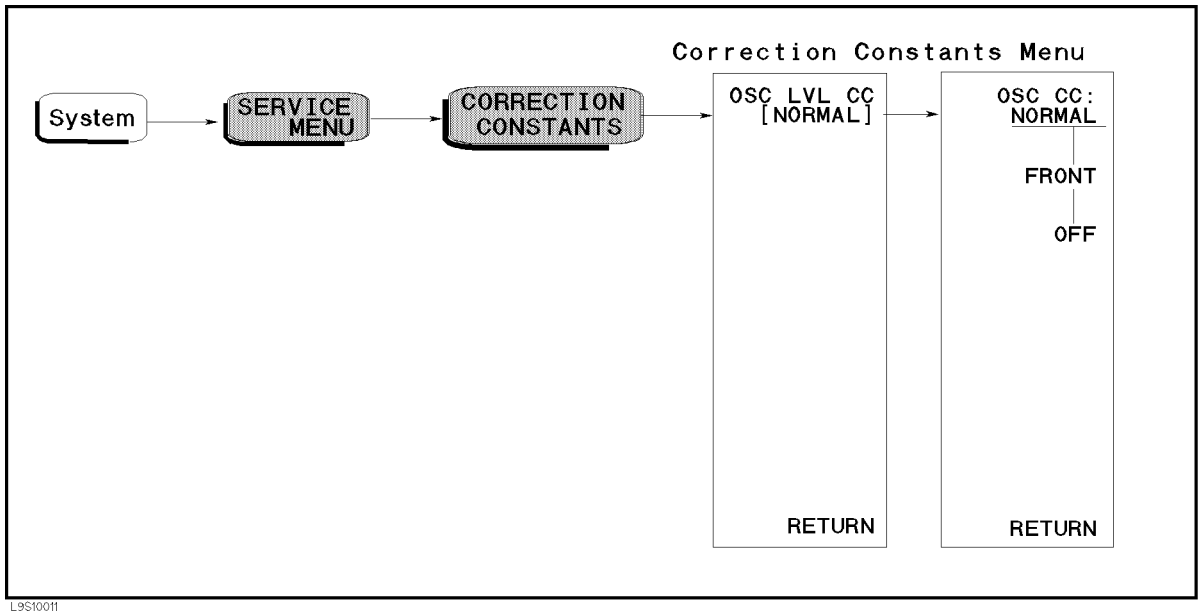


Figure 10-7. Correction Constants Menu

OSC LVL CC [ ] (:DIAG:SERV:CCON:OLEV {NORM|FRON|OFF})

Displays the control menu that allows you to select one of the OSC level correction constants settings of normal, front panel, and off. The softkeys in this control menu are described below. The abbreviation of the current setting is displayed in the brackets of the menu.

OSC CC: NORMAL	sets the OSC level correction constants to normal mode. In this mode, the OSC level setting applies to the measurement terminal.
FRONT	sets the OSC level correction constants to front panel mode. In this mode, the OSC level setting applies to the mainframe front "S" output.
OFF	sets the OSC level correction constants to off. In this mode, the OSC level is not corrected.

Note The corrections must be turned to on except when checking the analog circuits.

Correction Constants

The HP 4286A has the following correction constants in the EEPROM on the A1 CPU. It uses them to control the internal circuits and to achieve optimum performance by compensating for errors due to circuit characteristics. Each of the correction constants is described below. For the circuits that appear in the following description, see Chapter 11.

- **OSC Level Correction Constants** are control values for the level DAC in the A3A1 Source Vernier. These affect the OSC Level Accuracy.

SYNTHESIZER CONTROL MENU

Figure 10-8 shows the synthesizer control menus. To display the synthesizer control menu, press System, SERVICE MENU, SERVICE MODES, and SYNTH. Each softkey in the synthesizer control menu is described below.

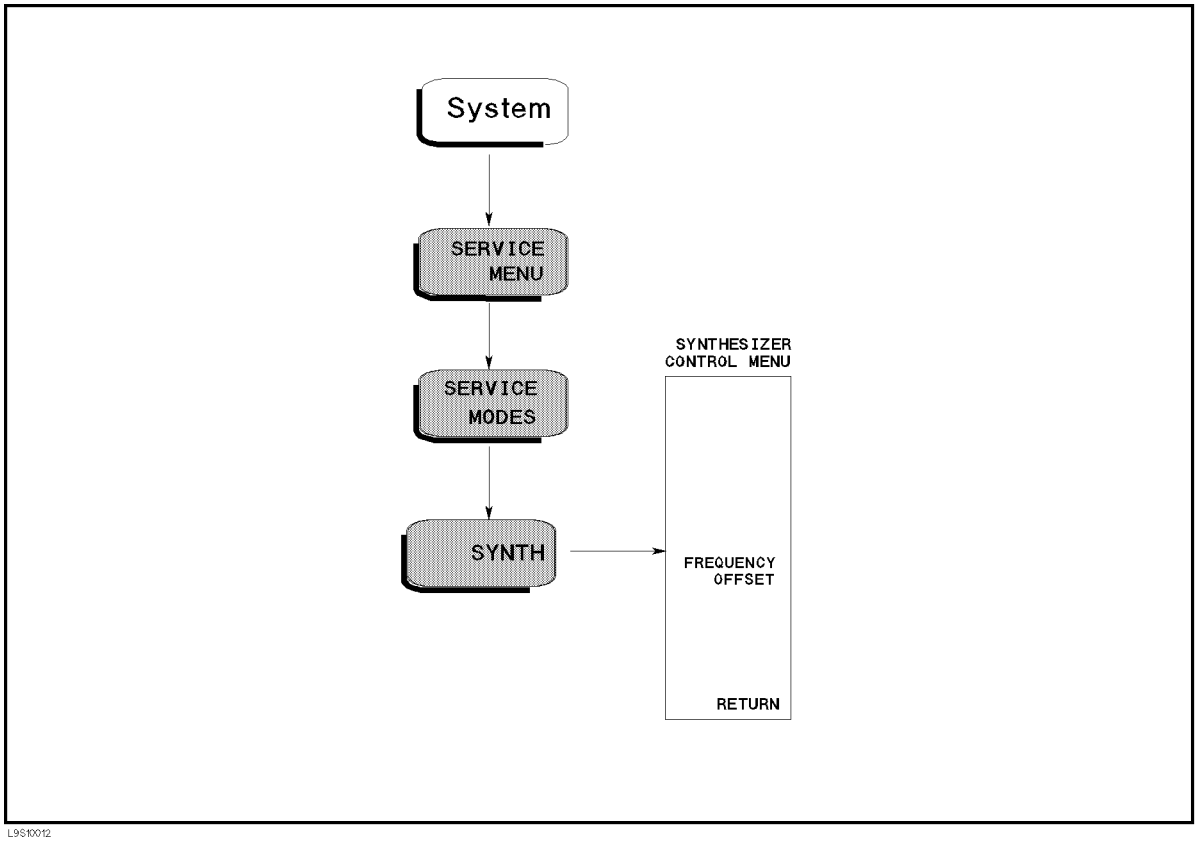


Figure 10-8. Synthesizer Control Menu

FREQUENCY OFFSET

(:DIAG:SERV:SYNT:FREQ:OFFS <*numeric*>)

Allows you to enter the frequency offset value. Factory use only.

OSC CONTROL MENU

Figure 10-9 shows the OSC control menu hierarchy. To display the OSC control menu, press (System), SERVICE MENU, SERVICE MODES, and OSC. Each softkey in the OSC control menus is described below.

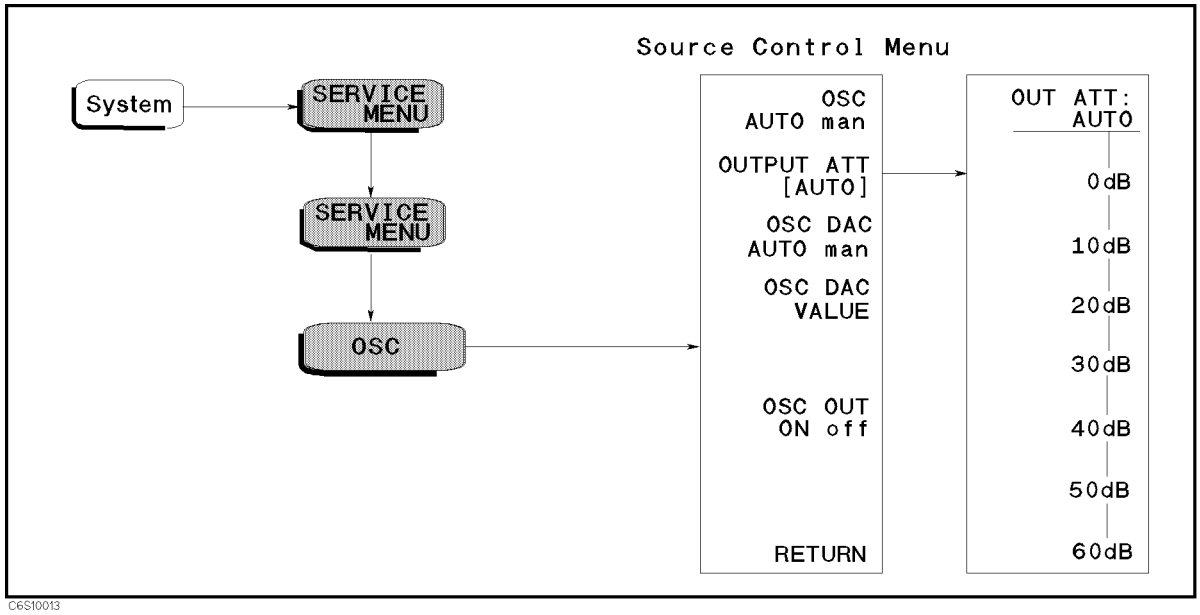


Figure 10-9. OSC Control Menu

OSC AUTO man (:DIAG:SERV:SOUR:MODE {AUTO|MAN})

Toggles the OSC control mode to automatic mode and manual mode. In the automatic mode, the HP 4286A sets the OSC level automatically according to the measurement settings. In the manual mode, the OSC level is controlled by the following softkeys.

OUTPUT ATT [ ] (:DIAG:SERV:SOUR:ATT {AUTO|DB0|DB10|DB20|DB30|DB40|DB50|DB60})

Displays the control menu that allows you to control the A7 output attenuator. The softkeys in this control menu are described below. The abbreviation of the current setting is displayed in the brackets of the menu.

`OUT ATT: AUTO` sets the A7 control to automatic mode. In this mode, the HP 4286A controls the A7 automatically according to the measurement setting.

`0 dB` sets the A7 output attenuator to 0 dB.

`10 dB` sets the A7 output attenuator to 10 dB.

`20 dB` sets the A7 output attenuator to 20 dB.

`30 dB` sets the A7 output attenuator to 30 dB.

`40 dB` sets the A7 output attenuator to 40 dB.

`50 dB` sets the A7 output attenuator to 50 dB.

`60 dB` sets the A7 output attenuator to 60 dB.

`OSC DAC AUTO man` (:DIAG:SERV:SOUR:LEV:DAC:MODE {AUTO|MAN})

Toggles the OSC DAC control mode in the A3A1 source vernier to automatic mode and manual mode. In the automatic mode, the HP 4286A sets the OSC DAC according the measurement settings. In the manual mode, the OSC DAC output is controlled by the `OSC DAC VALUE` softkey.

`OSC DAC VALUE` (:DIAG:SERV:SOUR:LEV:DAC:VAL <*numeric*>)

Allows you to enter the level DAC control value (0 to 32767). This value is used when the OSC DAC control mode is set to manual.

`OSC OUT ON off` (:DIAG:SERV:SOUR:STAT {OFF|ON|0|1})

Toggles the OSC switch in the A3A1 source vernier to turn on and off the OSC signal.

Note All settings must be turned to auto except when checking the analog circuits.

TRANSDUCER CONTROL MENU

Figure 10-10 shows the transducer (test head) control menu hierarchy. To display the TRD control menu, press System, SERVICE MENU, SERVICE MODES, and TRD.

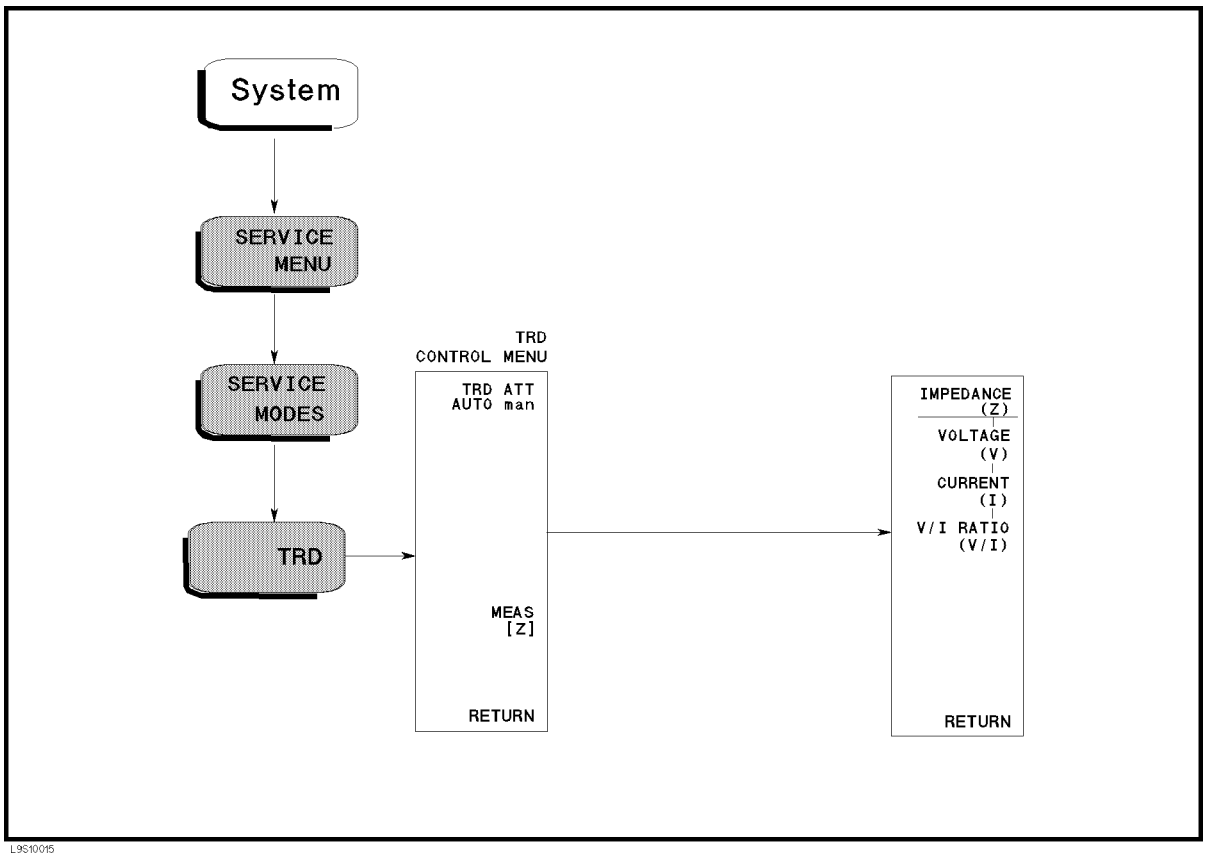


Figure 10-10. TRD Control Menu

MEAS [ ] (:DIAG:SERV:TRAN:SENS:FUNC {IMP|VOLT|CURR|VIR})

Displays the control menu that allows you to select display parameter from impedance, voltage, current, and voltage divided by current. The softkeys in this control menu are described below. The abbreviation of the current setting is displayed in the brackets of the menu.

IMPEDANCE (Z) sets the display parameter to impedance.

VOLTAGE (V) sets the display parameter to voltage.

CURRENT (I) sets the display parameter to current.

V/I RATIO (V/I) sets the display parameter to voltage divided by current.

IF CONTROL MENU

Figure 10-11 shows the IF control menu hierarchy. To display the IF control menu, press System, SERVICE MENU, SERVICE MODES, and IF. A softkey in the IF control menu displays one of menus used to control one of the A6 receiver IF circuits. Each softkey in the IF control menu is described below.

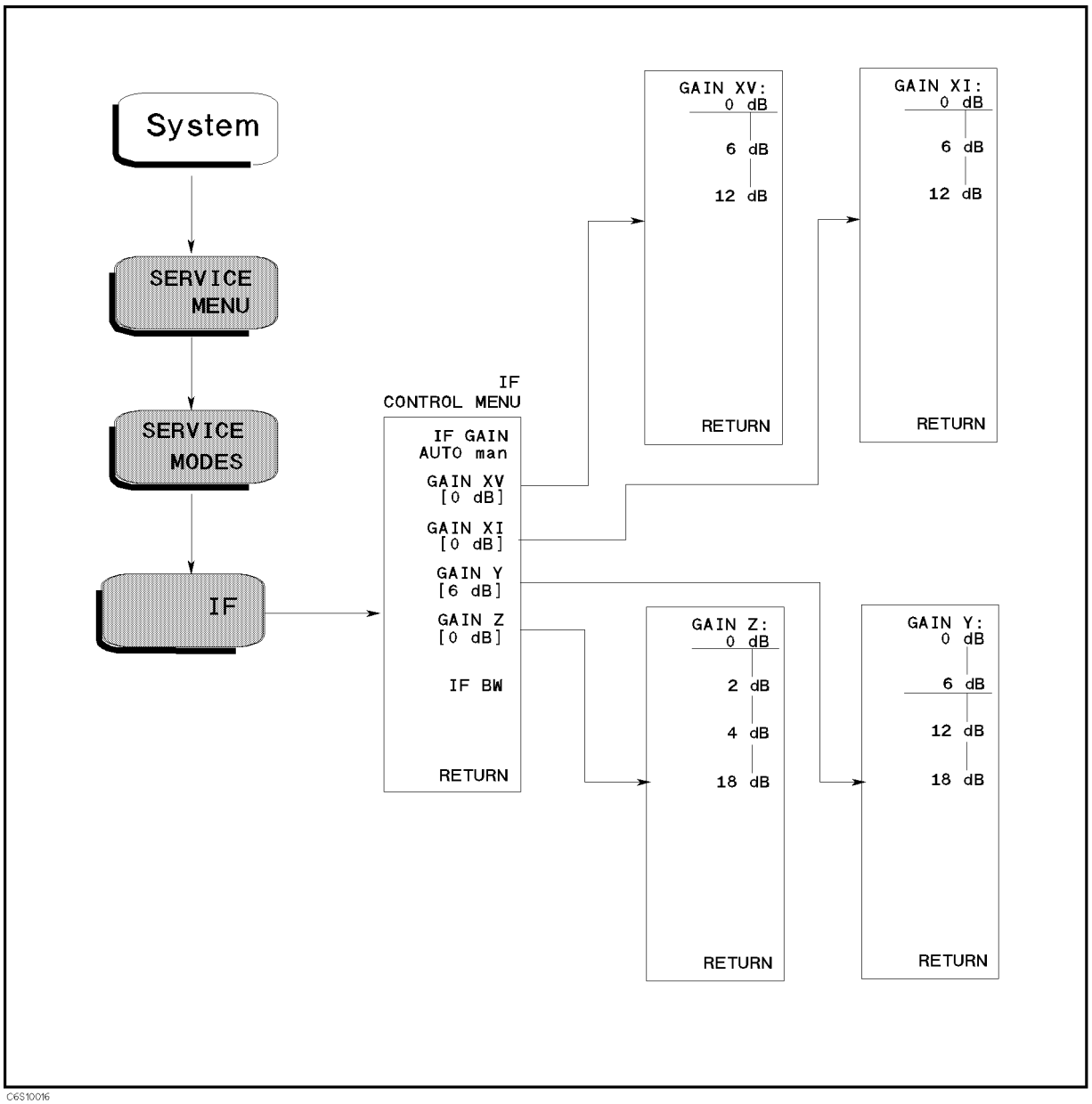


Figure 10-11. IF Control Menu

IF GAIN AUTO man (:DIAG:SERV:IF:GAIN:MODE {AUTO|MAN})

Toggles the IF gain control mode to automatic mode (normal operation) or manual mode. In the automatic mode, the HP 4286A controls the IF gain XV, XI, Y, and Z settings automatically according to the measurement setting. In the manual mode, the IF gains are controlled by the following softkeys.

GAIN XV [ ] (:DIAG:SERV:IF:GAIN:X:XV {DB0|DB6|DB12})

Displays the control menu for the IF GAIN XV (IF gain X in voltage measurement.) The softkeys in this control menu are described below. The abbreviation of the current setting (0 dB, 6dB, or 12 dB) is displayed in the brackets of the menu.

GAIN XV: 0dB	sets the IF GAIN XV to 0 dB.
6 dB	sets the IF GAIN XV to 6 dB.
12 dB	sets the IF GAIN XV to 12 dB.

GAIN XI [ ] (:DIAG:SERV:IF:GAIN:X:XI {DB0|DB6|DB12})

Displays the control menu for the IF GAIN XI (IF gain X in current measurement.) The softkeys in this control menu are described below. The abbreviation of the current setting (0 dB, 6dB, or 12 dB) is displayed in the brackets of the menu.

GAIN XI: 0dB	sets the IF GAIN XI to 0 dB.
6 dB	sets the IF GAIN XI to 6 dB.
12 dB	sets the IF GAIN XI to 12 dB.

GAIN Y [ ] (:DIAG:SERV:IF:GAIN:Y {DB0|DB6|DB12|DB18})

Displays the control menu for the IF GAIN Y. The softkeys in this control menu are described below. The abbreviation of the current setting (0 dB, 6dB, 12 dB, or 18 dB) is displayed in the brackets of the menu.

GAIN Y: 0dB	sets the IF GAIN Y to 0 dB.
6 dB	sets the IF GAIN Y to 6 dB.
12 dB	sets the IF GAIN Y to 12 dB.
18 dB	sets the IF GAIN Y to 18 dB.

GAIN Z [ ] (:DIAG:SERV:IF:GAIN:Z {DB0|DB2|DB4|DB18})

Displays the control menu for the IF GAIN Z. The softkeys in this control menu are described below. The abbreviation of the current setting (0 dB, 2dB, 4 dB, or 18 dB) is displayed in the brackets of the menu.

GAIN Z: 0dB	sets the IF GAIN Y to 0 dB.
2 dB	sets the IF GAIN Y to 2 dB.
4 dB	sets the IF GAIN Y to 4 dB.
18 dB	sets the IF GAIN Y to 18 dB.

IF BW

Displays the IF band pass filter band width of 1 kHz.

Note All settings must be turned to auto except when checking the analog circuits.

BOOTLOADER MENU

Figure 10-12 shows the Bootloader menus and the associated menus. To display the menu, turning the HP 4286A on with pressing (Trigger) and (Preset). The Bootloader menu is used to install the firmware into the HP 4286A using a firmware diskette and the built-in FDD. Also these menus are used to make a system backup diskette. Each softkey in the Bootloader menus is described below.

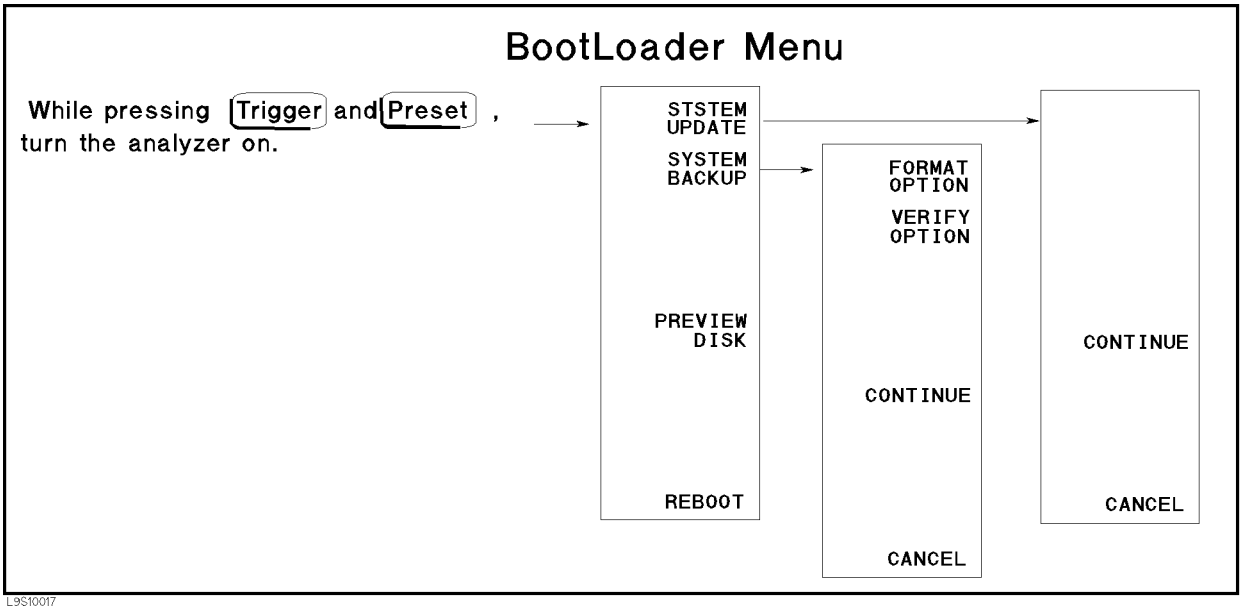


Figure 10-12. Bootloader Menu

SYSTEM UPDATE]

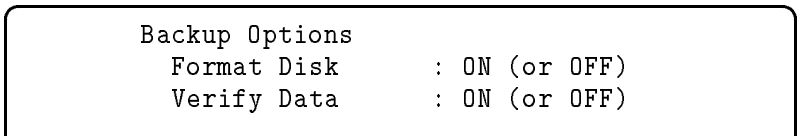
Allows you to install and update the firmware in the HP 4286A. Before pressing this softkey, insert the firmware diskette into the FDD on the front panel. Then press this softkey to install the firmware from the diskette to the HP 4286A. The detailed procedure is provided in the *Firmware Installation* in chapter 14.

After pressing this softkey, CONTINUE and CANCEL softkeys appear on the display. Press CONTINUE to continue the firmware installation. Press CANCEL to cancel the firmware installation.

SYSTEM BACKUP

Displays the control menu that allows you to make a system backup diskette in which the current firmware is stored. The applicable diskette is a 3.5 inch 1.44 MByte flexible disk. The softkeys in the control menu are described below.

FORMAT OPTION — toggles format option on and off. When the format option is set to on, the flexible diskette is initialized before storing the firmware. When the format option is set to off, the diskette is not initialized. The default setting is on. The format option setting is displayed as shown below.



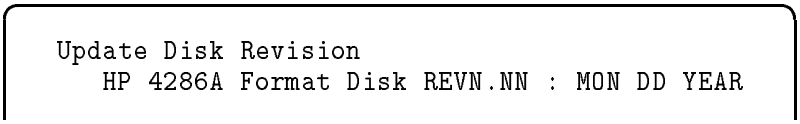
`VERIFY OPTION` toggles verify option on and off. When the verify option is set to on, the system stored in the flexible diskette is verified to be the same as the current firmware in the HP 4286A after storing the firmware. When the verify option is set to off, the verification is not performed. The default setting is on. The verify option setting is displayed as shown above.

`CONTINUE` continues making the system backup. Before pressing this softkey, insert a diskette into the FDD on the front panel.

`CANCEL` stops making the system backup and return to the Bootloader menu.

PREVIEW DISK

Displays the revision information of the firmware stored in the firmware diskette as shown below. Before pressing this softkey, insert a firmware diskette into the FDD on the front panel.



where N.NN: Revision Number
MON DD YEAR: Implementation Date (Month Day Year)

REBOOT

Reboots the HP 4286A. If the new firmware is installed, the HP 4286A boots up using the new firmware. After pressing the softkey, the HP 4286A performs the normal power on sequence.

11

Theory of Operation

The theory of operation begins with an overall description of the operation of the HP 4286A. The HP 4286A is divided into functional groups in the overall description, then the group descriptions follow.

The operation of each group is described for the purpose of assembly level repair. Detailed component-level circuit theory is not provided in this manual. See Figure 11-9 to Figure 11-12 to well understand the each group description.

OVERALL OPERATION

The HP 4286A consists of a mainframe, a test head, and a calibration kit (see Figure 11-1). The mainframe includes a source, a receiver, a digital control, and a power supply.

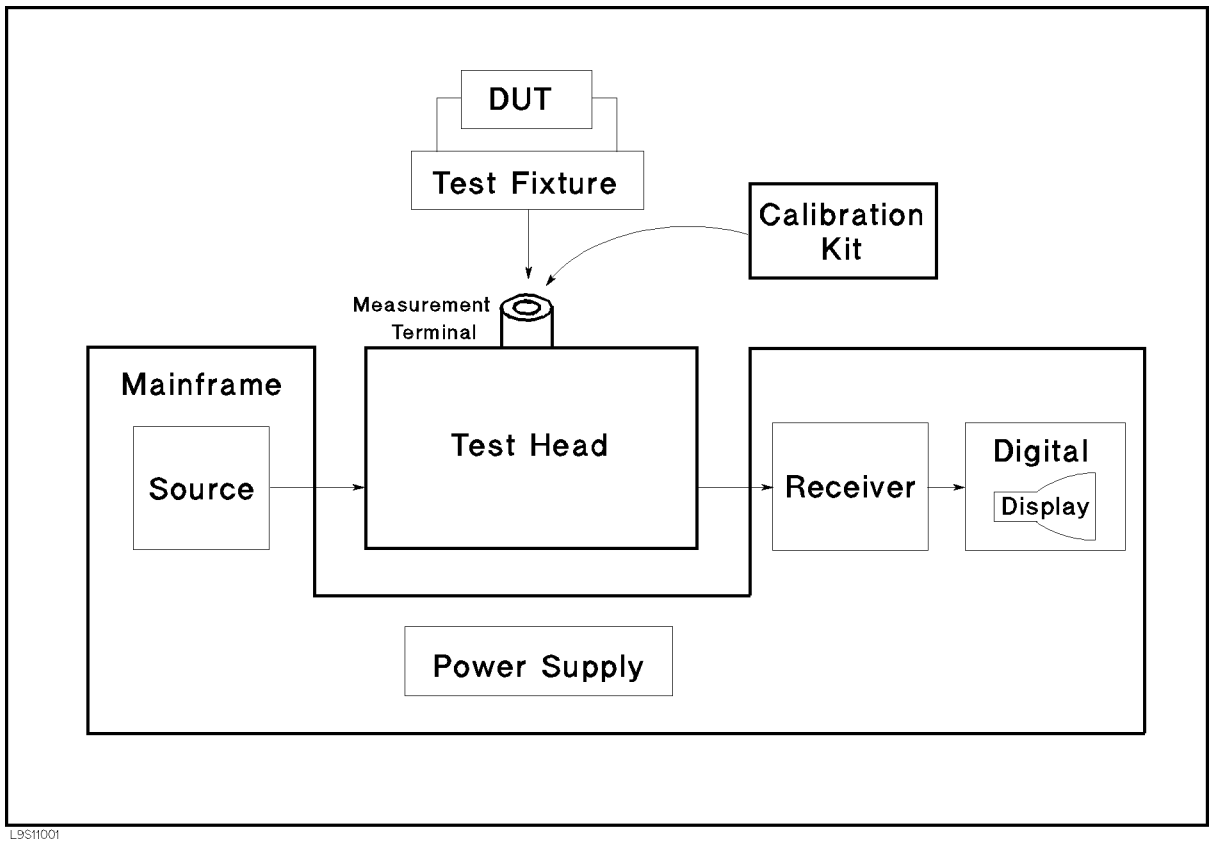


Figure 11-1. Simplified Block Diagram

The source generates a test signal in the range of 1 MHz to 1 GHz.

The test signal goes through the test head, and the test fixture to the device under test (DUT).

The test head senses the voltage across the DUT and the current through the DUT, and multiplexes the two signals and applies each signal to the receiver.

The receiver converts the signal to a digital signal, and forward it to the digital control.

The raw data is processed in the digital control. Then the processed data is routed to the CRT for display.

The calibration kit is used to calibrate the HP 4286A system. Calibration ensures the impedance measurement accuracy at the test head terminal.

The power supply in the mainframe supplies all necessary power for the HP 4286A.

FUNCTIONAL GROUPS

The HP 4286A consists of six main functional groups: a power supply, a digital control, a source, a receiver, a test head, and a calibration kit. Each group consists of several major assemblies, and performs a distinct function in the HP 4286A. (In fact, all the groups are interrelated to some extent and affect each other's performance.)

Power Supply: The power supply functional group consists of the A40 preregulator, the A2 post-regulator and the A52 DC-DC converter. It supplies power to the other assemblies in the HP 4286A.

Digital Control: The digital control group consists of the A1 CPU, the A30 keyboard, the A32 Instrument BASIC interface (option 1C2 only), the A33 handler interface, the A51 GSP (Graphics System Processor), the CRT display, and the Flexible Disk Drive. These assemblies combine to provide digital control for the HP 4286A.

Source: The source group consists of the A5 synthesizer, the A4A1 1st LO (1st local oscillator), the A3A1 level vernier, the A3A2 2nd LO (second local oscillator), the A3A3 source, and the A7 output attenuator. The source supplies a phase-locked test signal to the device under test, through the test head, and supplies the 1st and 2nd local oscillator signals to the receiver.

Receiver: The receiver group consists of the A4A2 receiver RF, and the A6 receiver IF. The receiver measures RF signal inputs, and forwards the measured data to the digital control.

Test Head: The test head group consists of the A43 head control and other test head assemblies. The test head interfaces the source and the receiver to the device under test to measure the device impedance.

Calibration Kit: The calibration kit consists of the open, short, 50 Ω and low-loss capacitor termination. The calibration kit is used to calibrate the HP 4286A.

The following pages describe the operation of the functional groups.

POWER SUPPLY OPERATION

The power supply functional group consists of the following assemblies:

- A40 Preregulator
- A2 Post-Regulator
- A52 DC-DC Converter

These assemblies comprise a switching power supply that provides regulated DC voltages to power all assemblies in the HP 4286A. See Figure 11-2.

The A40 preregulator steps down and rectifies the line voltage. It provides the following seven power supply voltages:

+70 V, +25 V, +18 V, +7.8 V, +5 VD, −7.8 V, −18 V

The +5 VD (+5 V digital supply) is fully regulated in A40 and is directly supplied to the A1 CPU. The other six power supplies are preregulated in A40 and go to the A2 post-regulator for final regulation.

A40 receives the FAN LOCK signal from the fan through the A20 motherboard and the A2 post-regulator.

The A2 post-regulator filters and regulates the six power supply voltages from A40. It distributes the following twelve regulated voltages to individual assemblies throughout the HP 4286A:

+65 V, FAN POWER (+24 V), +15 V, +15 V (AUX), +8.5, +5.3 V, +5 V, +5 V (AUX), −5 V, −12.6 V, −15 V

The A52 DC-DC converter converts the +65 V voltage supplied from the A2 post-regulator into the +15 V voltage to power the CRT display.

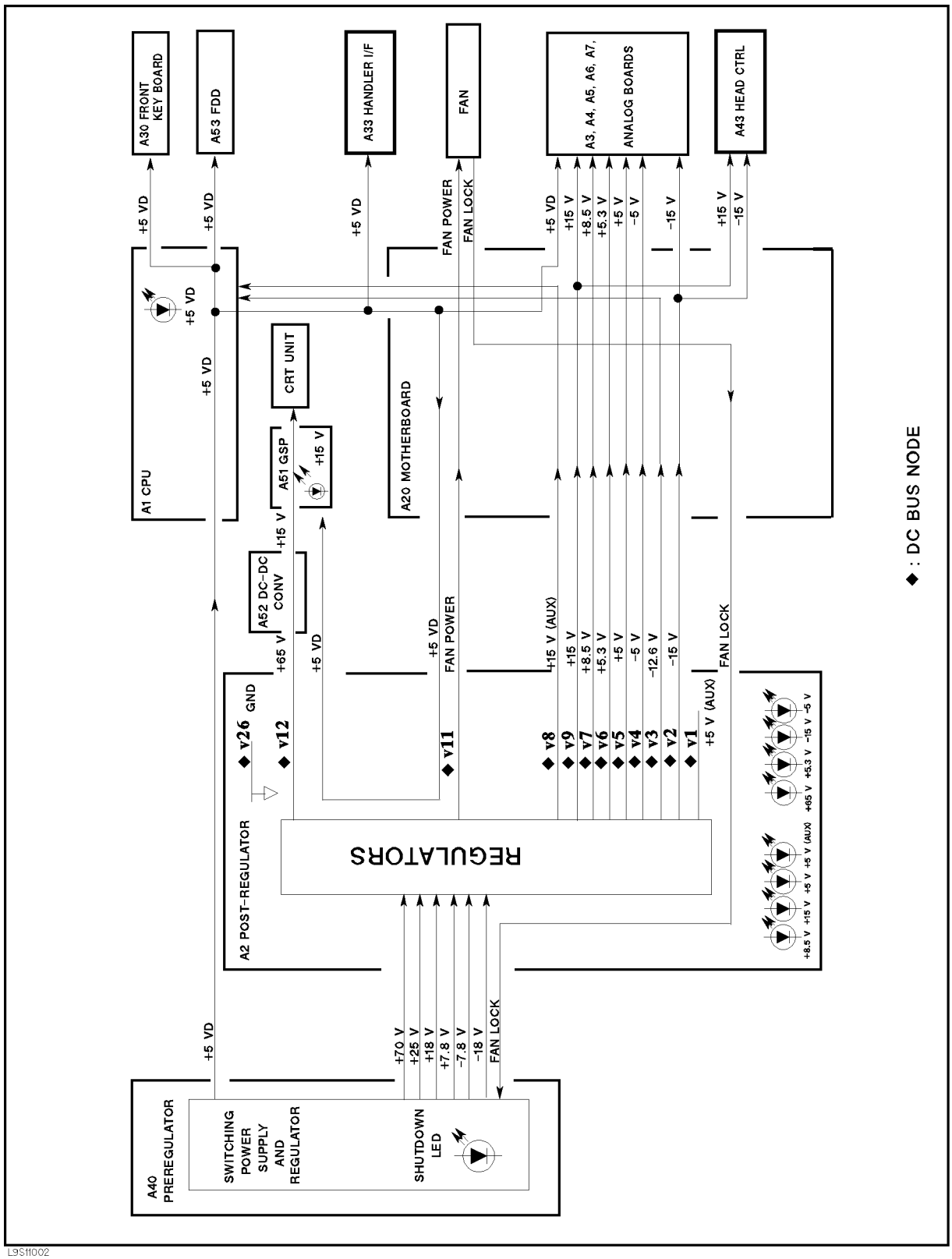


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Figure 11-2. Power Supply Functional Group, Simplified Block Diagram

A40 Preregulator

The A40 preregulator consists of the line power module and the two switching regulators (1 and 2). The preregulator provides an LED (visible at the top) to indicate circuit status.

Line Power Module

The line power module contains a line power switch that includes a main fuse and a rectifier that includes a voltage selector switch. The main fuse, which protects the input side of the preregulator from drawing too much line current, is also accessible at the rear panel. See *Power Requirements* in appendix B for the fuse replacement, the line voltage setting, and other power considerations.

Switching Regulator 1

Switching regulator 1 converts the line voltage to two DC voltages +70 V and +25 V. The partially regulated voltages are routed to the A2 post-regulator for final regulation.

Switching regulator 1 is equipped with an over voltage protection circuit. The circuit activates when an over voltage is sensed on the +70 V power line or when the FAN LOCK signal is sensed. It shuts down the +70 V and +25 V power supplies, which shuts down switching regulator 2. The A40 shutdown LED is turned on.

Switching Regulator 2

Switching preregulator 2 converts the line voltage to five DC voltages, +18 V, +7.8 V, +5 V for digital supply (+5 VD), −7.8 V, and −18 V. The regulated +5 VD goes directly to the A1 CPU. The other four partially regulated voltages are routed to the A2 post-regulator for final regulation.

Switching regulator 2 is equipped with an over voltage and over current protection circuit. The circuit activates when an over voltage is sensed on the +5 VD power line, when an over current is sensed on one of four power supplies (±18 V and ±7.8 V), or when the FAN LOCK signal is sensed. It shuts down all five power supplies of switching regulator 2.

The A40 shutdown LED is turned on when an over voltage on the +5 VD power line is sensed or the FAN LOCK signal is sensed. But, it does not shut down when an over current is sensed on the four power lines of ±18 V and ±7.8 V.

Regulated +5V Digital Supply (+5 VD)

The +5VD power supply is fully regulated in the A40 preregulator. It goes directly to the A1 CPU and is supplied to all assemblies requiring a digital +5 V supply through A1, the A20 motherboard, and the A2 post-regulator. See Figure 11-2.

For A40 to work properly, the +5 VD must be loaded by one or more assemblies. If it is not, the other preregulated voltages in the A40 preregulator will not be correct.

A40 Shutdown LED

The A40 shutdown LED is off during normal operation. It turns on when the A40 protective circuits are activated and shut down some power limes. The shutdown LED turns on when one of the following conditions is sensed:

- Over voltage on +70 V Power Line.
- Over voltage on +5 VD Power Line.
- Fan is not rotating (FAN LOCK signal is sensed).

Shutdown circuit 2 in Figure 5-14 shows that the shutdown LED turns on when an over voltage is sensed on the +5 VD power line or the FAN LOCK signal is sensed. In addition,

the shutdown LED turns on when an over voltage is sensed on the +70 V power line. When switching regulator 1 shuts down due to an over voltage on the +70 V power line, the fan is stopped because the +25 V power is missing. The fan obtains its power from the +25 V power line through the A2 post-regulator. Then, the FAN LOCK signal shuts switching regulator 2 down and turns the A40 shutdown LED on.

A2 Post-Regulator

The A2 post-regulator consists of eight filters, ten regulators, and the drive circuits for the A7 output attenuator and the A8 input attenuator.

The A2 post-regulator distributes the following nine power supply voltages to individual assemblies throughout the HP 4286A. Each of the ten regulators receives the DC voltage preregulated in A40 through a filter and converts it to one of the fully regulated constant DC voltages listed below:

+65 V	is derived from the +70 V supply from A40. It is converted to +15 V at the A52 DC-DC converter.
FAN POWER	is derived from the +25 V supply from A40 and is typically +24 V. It powers the fan.
+15 V	is derived from the +18 V supply from A40. It powers analog assemblies A3 through A9, and A43.
+8.5 V	is derived from the +15 V supply regulated in the A2 post-regulator. It powers the A3A3 source.
+5.3 V	is derived from the +7.8 V supply from A40. It powers the A3A3 source.
+5 V	is derived from the +7.8 V supply from A40. It powers analog assemblies A3 through A9.
+5 V (AUX)	is derived from the +25 V or +18 V supplies from A40. It powers A2.
–5 V	is derived from the –7.8 V supply from A40. It powers analog assemblies A3 through A9.
–15 V	is derived from the –18 V supply from A40. It powers analog assemblies A3 through A9, and A43.

The A2 post-regulator is equipped with a protective shutdown circuit.

The A2 post-regulator provides two LED arrays, visible at the top edge of the A2 post-regulator. Each LED array consists of four LEDs and indicates status of eight power supplies.

Shutdown Circuit

Five regulators for power supplies, +65 V, +15 V, +5 V, –5 V, and –15 V are equipped with the capability of sensing over current, and over voltage, under voltage on their output lines. When a regulator senses one of these conditions, it triggers the protective shutdown circuit. The circuit is also triggered by an over temperature condition in A2. Table 11-1 shows the power supplies that are shut down.

Table 11-1. Shutdown Operation

Power Supply	Trouble on +65 V	Trouble on ±15 V and ±5 V	Over-temperature
+65 V	√		
+15 V	√	√	√
+8.5 V	√	√	√
+5.3 V	√	√	√
+5 V	√	√	√
−5 V	√	√	√
−15 V	√	√	√

The following power supplies are not shutdown:

FAN POWER, +22 V, +12.6 V, +15 V (AUX), +5 V (AUX)

The shutdown circuit also provides the shutdown status to the A1 CPU. When the circuit is activated, it triggers the A1 CPU. The A1 CPU checks the shutdown status on the A2 post-regulator and displays a warning message. Then the HP 4286A stops its operation. Once the HP 4286A stops the operation, the front-panel keys are disabled. The only way to reset the HP 4286A is to turn the HP 4286A power off then on.

Eight Status LEDs

The eight status LEDs on the A2 post-regulator are on during normal operation. They indicate that the correct voltage is present in each supply. See Figure 11-3. If one (or more) LED is off or flashing, there is a problem in the corresponding power supply.

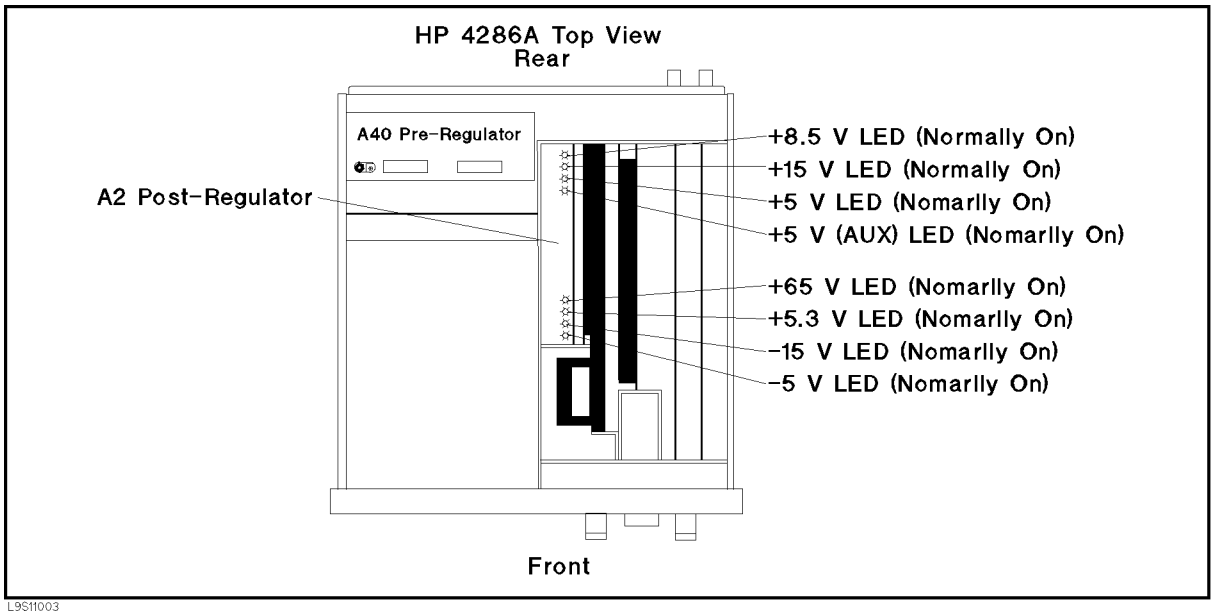

Figure 11-3. A2 Eight Status LED

A7 Output Attenuator Drive Circuit

The A2 post-regulator has the drive circuit for the A7 output attenuator. The circuit decodes the control signal from the A1 CPU and supplied the following signal to A7 through the A20 motherboard:

- A7 input attenuator drive signals (10 dB ON/OFF, 20 dB ON/OFF, 30 dB ON/OFF).

A52 DC-DC Converter

The A52 DC-DC converter converts the +65 V voltage supplied from the A2 post regulator into the +15.75 V voltage. The output voltage is supplied to the A51 GSP and the monochrome CRT display.

DIGITAL CONTROL OPERATION

The digital control functional group consists of the following assemblies:

- A1 CPU
- A30 Front Keyboard
- A31 Interface Connector
- A32 I-BASIC Interface (Option 1C2 only)
- A33 Handler Interface / Backup SRAM
- A51 GSP
- CRT Display
- FDD (Flexible Disk Drive)

These assemblies combine to provide digital control for the HP 4286A. They provide math processing functions, as well as communications between the HP 4286A and an external controller and/or peripherals. Figure 11-4 is a simplified block diagram of the digital control functional group.

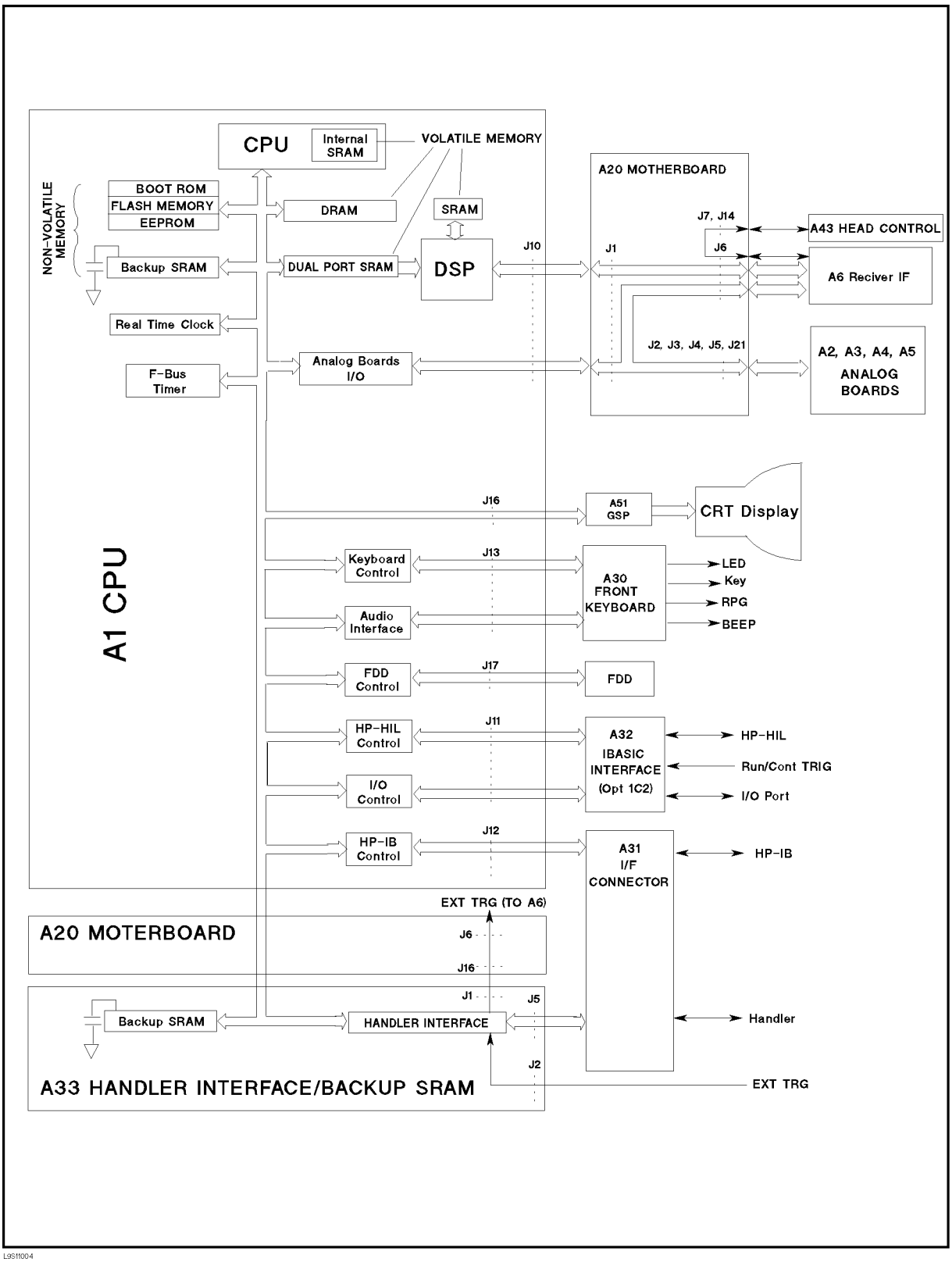

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Figure 11-4. Digital Control Group, Simplified Block Diagram

A1 CPU

The A1 CPU consists of the following circuits and parts (See Figure 11-4):

CPU	central processing unit that controls the HP 4286A.
DSP	digital signal processor that is used for fast data processing.
Memory Storages	consists of BOOT ROMs, Flash Memory, EEPROM, Backup SRAM, DRAM, and Dual Port SRAM. The backup SRAM is powered from a large capacitor that is charged when the analyzer is turned on. Therefore, the SRAM keeps its data at least 72 hours after the analyzer is turned off. The Dual Port SRAM is used for communication between the CPU and DSP.
F-Bus Timer	is used in the frequency bus measurement that is a diagnostic function of the analyzer. For a description of the frequency bus measurement, see Chapter 10.
Analog Board Interface	interfaces between the CPU and analog assemblies A3 through A9
Keyboard Controller	controls the A30 front-panel keyboard.
Audio Interface	controls the beeper on the A30 front-panel keyboard.
FDD Control	controls the Floppy Disk Drive.
HP-IB Control	communicates with the external HP-IB devices through the HP-IB connector on the A31 interface connector.
HP-HIL Control	interfaces between the CPU and the external keyboard through the HP-HIL connector on the A32 I-BASIC Interface.
I/O Control	controls the external devices through the I/O PORT connector on the A32 IBASIC interface. It also interfaces between the CPU and the external inputs through the EXT PROG RUN/CONT connector.

A30 Front-Panel Keyboard

The A30 front-panel keyboard assembly detects your key inputs from the front panel of the HP 4286A, and transmits them to the keyboard controller on A1.

A31 Interface Connector

The A31 assembly consists of the HP-IB interface connector and the handler interface connector. The A31 assembly is connected to the HP-IB control circuit on A1 (through the A20 motherboard) and the A33 handler interface.

A32 I-BASIC Interface (Only for Option 1C2)

The three A32 I/O connectors are the EXT PROG RUN/CONT connector, the I/O Port connector, and the HP-HIL connector. These connectors are connected to the I/O control and HP-HIL control circuit on A1 through the A20 motherboard. The A32 assembly is only installed in an analyzer equipped with option 1C2.

A33 Handler Interface / Backup SRAM

The A33 assembly has the following two functions:

Handler Interface	interfaces the HP 4286A to an external handler through the A31 interface connector. The interface input/output signal is opto-isolated.
Backup SRAM	is powered from a large capacitor that is charged when the analyzer is turned on, and the SRAM keeps its data at least 72 hours after the analyzer is turned off. In this backup SRAM, the calibration/compensation data is stored with (Save/Recall) function.

A51 GSP

The A51 Graphics System Processor provides the interface between the A1 CPU and the CRT display. The A1 CPU converts the formatted data into GSP commands and writes them to the A51 GSP. The A51 GSP processes the data to obtain the necessary video signals and sends these signals to the CRT display

CRT Display

The CRT display is a monochrome CRT with associated drive circuitry.

Flexible Disk Drive

The HP 4286A has a built-in, 3-1/2 inch FDD (Flexible Disk Drive) on the front panel. It uses 2 high density or 2 double density 3-1/2 inch flexible disks. The FDD stores and retrieves data to and from the disk.

SOURCE THEORY

The two functional subgroups of the source group are the synthesizer and the stimulus.

The synthesizer subgroup generates the 40 MHz reference frequency, the 1st local oscillator signal (2.05958 GHz to 3.05858 GHz), and the second local oscillator signal (2.08 GHz). These signals are used in both the stimulus signal subgroup in the source functional group and in the receiver functional group.

The stimulus subgroup generates a stable and accurate test signal between 1 MHz to nobreak|1 GHz| with a power level from -33 dBm to +7 dBm.

Figure 11-5 shows the simplified block diagram of the source functional group. The source group consists of the following assemblies:

- A5 Synthesizer
- A4A1 1st LO
- A3A1 Source Vernier
- A3A2 2nd LO
- A3A3 Source
- A7 Output Attenuator

The first three assemblies and part of the A3A2 2nd LO belong to the synthesizer subgroup. The next four assemblies belong to the stimulus subgroup. A3A2 contains the second local oscillator and the source first mixer. The second local oscillator is part of the synthesizer subgroup. The source first mixer is part of the stimulus subgroup.

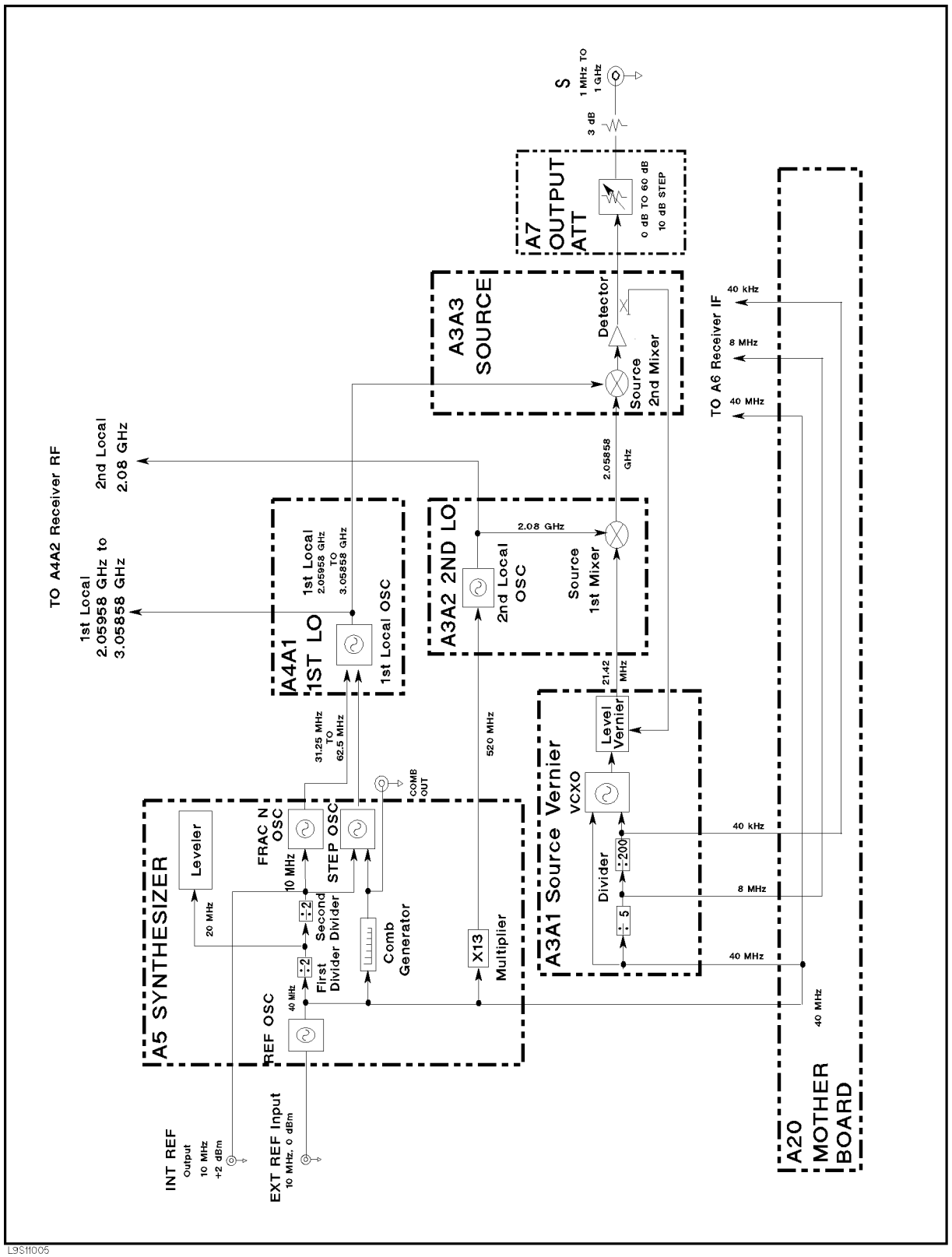

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Figure 11-5. Source Simplified Block Diagram

A5 Synthesizer

The A5 synthesizer provides a 40 MHz reference frequency, an INT REF signal, a FRAC N OSC signal, and a 520 MHz signal.

The 40 MHz reference signal is supplied to the A3A1 level vernier and the A6 receiver IF and is used as the reference signal. The FRAC N OSC signal is supplied to the A4A1 1st LO and used to generate the 1st local oscillator signal. The 520 MHz signal is supplied to the A3A2 2nd LO and is used to generate the second local oscillator signal.

The A5 Synthesizer consists of the following circuits:

- REF OSC (Reference Oscillator)
- FRAC N OSC (Fractional N Oscillator)
- STEP OSC (Step Oscillator)
- X 13 Multiplier

REF OSC

The REF OSC generates stable 10 MHz and 40 MHz reference frequencies. It does this by dividing the output of a 40 MHz VCXO (voltage control crystal oscillator) as required. The 40 MHz reference signal is supplied to the A3A1 level vernier. The 10 MHz reference frequency is routed to the INT REF Output connector on the rear panel.

When a 10 MHz external reference signal is applied to the EXT REF Input connector on the rear panel, the REF OSC output signals are phase locked to the external reference signal.

The REF OSC is a phase locked oscillator and contains a 40 MHz VCXO, a phase detector, and three 1/2 dividers. See Figure 11-9. When the 10 MHz external reference signal is applied to the EXT REF Input connector on the rear panel, the reference frequency is divided by two. It is then compared with the VCXO frequency ($\mathbf{F_{vcxo}}$) divided by eight in the phase detector. Phase locking imposes the condition of 10 MHz/2 = $\mathbf{F_{vcxo}}$/8. Therefore, the output frequency ($\mathbf{F_{vcxo}}$) is locked to 40 MHz.

A detector circuit detects the external reference input signal and sends the status to the A1 CPU. Then the A1 CPU displays a message (**ExtRef**) on the CRT. In addition, an unlock detector monitors the control voltage to the VCXO. When the control voltage is out of limits, the detector sends the status to the A1 CPU. Then the A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

The *40 MHz Reference Oscillator Frequency Adjustment* adjusts the VCXO to lock to the 40 MHz when the external reference signal is not applied.

FRAC N OSC

The FRAC N OSC (Fractional N Oscillator) generates a signal of 31.25 MHz to 62.5 MHz with a high frequency resolution. The signal is supplied to the A4A1 1st LO and is used to generate the 1st local oscillator signal.

The FRAC N OSC is a phase locked oscillator. The output signal is phase locked to the 10 MHz reference signal of the REF OSC. The oscillator contains a 31.25 MHz to 62.5 MHz VCO, a phase detector, and a fractional N divider (N.F. divider: 1/**in**teger.**f**raction). See Figure 11-9.

The 10 MHz reference signal from the REF OSC is applied to the phase detector through the 1/10 divider. The reference signal is then compared with the VCO frequency ($\mathbf{F_{vco}}$) divided by the fractional N divider in the phase detector. Phase locking imposes the condition of 10 MHz/10 = $\mathbf{F_{vco}}$/N.F. Therefore, the output frequency ($\mathbf{F_{vco}}$) is locked to 1 MHz × N.F.

The fractional N divider is a dedicated divider used to generate the high frequency resolution signal. It divides the signal frequency by a real value (N.F.). The resolution of the fractional part F is 3.55×10^{-15} (= $1/2^{48}$). Therefore, the FRAC N OSC generates a signal with 3.55 nHz

(1 MHz × 3.55 × 10^{-15}) frequency resolution. The fractional N divider is controlled by the A1 CPU and the A6 Receiver IF.

STEP OSC

In the HP 4286A, the output signal of this circuit is not used.

Multiplier (X 13)

The multiplier receives the 40 MHz reference signal and generates a 520 MHz signal. This signal is supplied to A3A2 2nd LO and is used to generate the second local oscillator signal. See Figure 11-9. The 520 MHz signal level is adjusted in the *520 MHz Level Adjustment*.

A4A1 1st LO

The A4A1 1st LO generates the 1st local oscillator signal of 2.05958 GHz to 3.05858 GHz with 1 mHz resolution.

The 1st local oscillator signal is supplied to the A3A3 source and the A4A2 receiver RF. In A3A3, the local oscillator signal is used to convert the 2.05858 GHz IF (intermediate frequency) signal to the 1 MHz to 1 GHz RF signal. A4A2 also uses the first local to convert the RF input signal to the IF signal.

In addition, the A4A1 1st LO decodes two digital control signals for the A4A2 Receiver RF, and the decoded signals are supplied to A4A2.

1st Local OSC Circuit

The 1st local oscillator circuit is a phase locked oscillator. The output signal is phase locked to the FRAC N OSC output signal. The oscillator contains a 2.05958 GHz to 3.05858 GHz VCO, a phase detector, a 1/4 divider, a mixer, a 1/16 divider, and a single/triple switch. See Figure 11-10.

In the HP 4286A, the single/triple switch is always set to the single-loop mode.

An unlock detector monitors the control voltage to the VCO. When the control voltage is out of the limits, the detector sends the status to the A1 CPU. The A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

Single-Loop Operation. In the single-loop mode, the VCO signal loops back to the phase detector through the 1/4 divider and the 1/16 divider. The VCO frequency ($\mathbf{F_{vco}}$) is divided by 64 and then compared with the FRAC N OSC signal frequency ($\mathbf{F_{frac}}$) (31.25 MHz to 62.5 MHz) in the phase detector. Phase locking imposes the condition of $\mathbf{F_{frac}} = \mathbf{F_{vco}}$ /64. Therefore, the output frequency ($\mathbf{F_{vco}}$) is locked to $\mathbf{F_{frac}} \times 64$. The $\mathbf{F_{vco}}$ sweeps from 2 GHz (31.25 MHz × 64) to 4 GHz (62.5 MHz × 64) according to the FRAC N OSC; swept signal. The frequency range actually used in the analyzer is 2.05958 GHz (at a measurement frequency 1 MHz) to 3.05858 GHz (at a measurement frequency 1 GHz).

A3A1 Source Vernier

The A3A1 source vernier generates the level-controlled 21.42 MHz IF signal, an 8 MHz reference signal, and a 40 kHz reference signal.

The 21.42 MHz signal is supplied to the A3A2 2nd LO and converted to a 2.05858 GHz IF signal through the source first converter. The 8 MHz and 40 kHz signals are supplied to the A6 receiver IF and used as reference signals.

The A3A1 level vernier consists of the following circuits:

- Divider

- Source Oscillator
- Level Vernier

Divider

The divider contains a 1/5 divider and a 1/200 divider. The 40 MHz reference frequency from the A5 synthesizer is down converted to 8 MHz and 40 kHz through the two dividers. The two signals are then supplied to the A6 receiver IF through the A20 motherboard.

Source OSC

The source OSC (source oscillator) is a phase locked oscillator. The output signal is phase locked to the 40 kHz frequency of the divider output. The oscillator generates the 85.68 MHz signal. The signal is divided by the 1/4 divider. The resulting 21.42 MHz signal is supplied to the level vernier circuit.

The oscillator contains an 85.68 MHz VCXO, a phase detector, a 1/2 divider, a mixer, and a 1/71 divider. See Figure 11-9. The VCO frequency ($\mathbf{F_{vco}}$) is divided by 2 and mixed with the 40 MHz reference frequency in the mixer. The mixer then produces a shifted frequency ($\mathbf{F_{vco}}/2 -$ 40 MHz). The mixer output is divided by 71 and then compared with the 40 kHz reference signal in the phase detector. Phase locking imposes the condition of 40 kHz = ($\mathbf{F_{vco}}/2 -$ 40 MHz)/71. Therefore, the output frequency ($\mathbf{F_{vco}}$) is locked to 85.68 MHz (= (40 kHz × 71 + 40 MHz) × 2).

The VCXO is optimized by the "Source VCXO Adjustment."

Level Vernier

The level vernier controls the level of the 21.42 MHz signal from the source OSC. The signal is routed to the output connector on the front panel through the A3A2 2nd LO, the A3A3 source, and the A7 Output Attenuator.

The level vernier consists of a level DAC and a level vernier. See Figure 11-9.

The level vernier changes the 21.42 MHz signal level according to the DAC output level. The DAC output level is set according to the predefined data in the EEPROM on the A1 CPU. The data is stored by performing the *Osc Level Correction Constants*.

A3A2 2nd LO

The A3A2 2nd LO generates the second local oscillator signal (a 2.08 GHz signal) and converts the 21.42 MHz signal from the A3A1 level vernier to a 2.05858 GHz IF signal by mixing the 21.42 MHz and the second local oscillator signal.

The 2.05858 GHz IF signal is supplied to the A3A3 source and then converted to a RF signal. The second local oscillator signal is supplied to the A4A2 receiver RF.

The A3A2 2nd LO consists of the following circuits:

- 2nd LO
- Source First Mixer

2nd LO

The 2nd Local oscillator circuit is a phase locked oscillator. The output signal is phase locked to the 520 MHz frequency from the A5 synthesizer. The oscillator generates a 2.08 GHz signal. The signal is supplied to the source first mixer and the A4A1 receiver RF.

The oscillator contains a 1.04 GHz VCO, a phase detector, and a 1/2 divider. See Figure 11-10. The VCO frequency ($\mathbf{F_{vco}}$) is divided by 2 and then compared with the 520 MHz reference signal

in the phase detector. Phase locking imposes the condition of 520 MHz = $\mathbf{F_{vco}}/2$. Therefore, the output frequency ($\mathbf{F_{vco}}$) is locked to 1.04 GHz (= 520 MHz × 2). Then the signal frequency is converted to 2.08 GHz by the doubler.

The 520 MHz reference signal contains 40 MHz harmonics because it is generated by multiplying the 40 MHz reference signal in the A5 synthesizer. The *Second Local PLL Adjustment* adjusts the 2nd LO to lock to the 520 MHz harmonic, rather than the neighboring harmonics (480 MHz or 560 MHz).

An unlock detector monitors the control voltage to the VCO. When the control voltage is out of the limits, the detector sends the status to the A1 CPU. The A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

Source First Mixer

The 21.42 MHz signal from the A3A1 level vernier is mixed with the 2.08 GHz second local oscillator signal through the first source mixer. Then the signal is converted to a 2.05858 GHz signal through the BPF (band pass filter). The 2.05858 GHz signal is supplied to the A3A3 source.

A3A3 Source

The A3A3 source generates a stable and accurate RF signal of 1 MHz to 1 GHz, with a power level from -10 dBm to +20 dBm. The RF signal is supplied to the A7 output attenuator. The A3A3 source consists of the following circuits (see Figure 11-10):

- Source Second Mixer
- Source Amplifier
- Level Detector

The 2.05858 GHz IF signal from the A3A2 2nd LO is applied to the source second mixer. It is then converted to the RF signal (1 MHz to 1 GHz) by mixing with the 1st local oscillator signal (2.05958 GHz to 3.05858 GHz) from the A4A1 1st LO. The RF signal is amplified with a constant gain through the source amplifier. It is then supplied to the A7 output attenuator through the level detector. The level detector loops the RF signal level back to the A3A1 level vernier.

A7 Output Attenuator

The A7 output attenuator is a 10 dB step attenuator from 0 dB to 60 dB. A7 consists of three segments (10 dB, 20 dB, and 30 dB). Attenuation from 0 dB to 60 dB is obtained by combining one (or more) of the three segments. Each segment is activated by the TTL signals from the A2 post-regulator.

Table 11-2 shows the relationship between the oscillator level setting and the A7 setting.

Table 11-2. Osc Level Setting vs. A7 Output Attenuator Setting

Osc Level	A7 Attenuation
0.22 Vrms < Osc ≤ 1.0 Vrms[1]	0 dB
70 mVrms < Osc ≤ 0.22 Vrms	10 dB
22 mVrms < Osc ≤ 70 mVrms	20 dB
7.0 mVrms < Osc ≤ 22 mVrms	30 dB
2.2 mVrms < Osc ≤ 7.0 mVrms	40 dB
0.70 mVrms < Osc ≤ 2.2 mVrms	50 dB
0.20 mVrms < Osc ≤ 0.70 mVrms	60 dB

1 Osc ≤ 0.5 Vrms for frequency > 1 GHz

RECEIVER THEORY

The receiver receives the RF signal from the test head and converts the signal to digital data. The RF signal is converted to the 1st IF (intermediate frequency), then to 2nd IF, and finally to the 3rd IF. The 3rd IF is converted to a digital signal using A/D converter.

Figure 11-6 shows the simplified block diagram of the receiver functional group. The receiver group consists of the following assemblies:

- A4A2 Receiver RF
- A6 Receiver IF

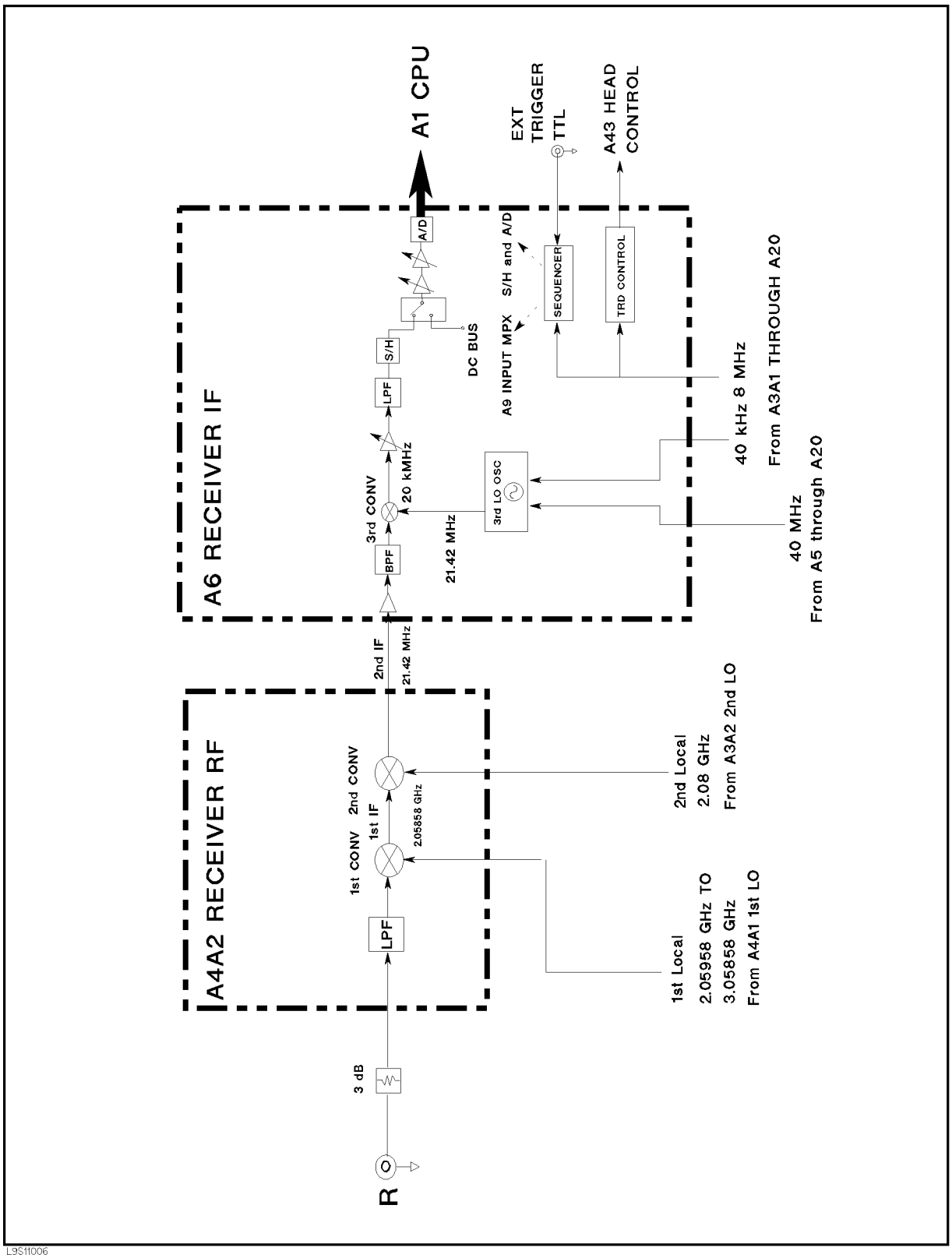

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Figure 11-6. Receiver Simplified Block Diagram

A4A2 Receiver RF

The A4A2 receiver RF converts the RF input signal from the test head to the 21.42 MHz 2nd IF. The 2nd IF is routed to the A6 receiver IF.

The A4A2 receiver RF consists of the following circuits (See Figure 11-11):

- 1st Converter
- 2nd Converter

In the first converter, the RF signal (1 MHz to 1 GHz) is mixed with the 1st local oscillator signal (2.05958 GHz to 3.05858 GHz) from A4A1 and then converted to the 2.05858 GHz 1st IF through the band pass and low pass filters.

In the second converter, the 1st IF is mixed with the 2.08 GHz second local oscillator signal from A3A2. This converts it to the 21.42 MHz second IF through the low pass filters.

The second IF signal is routed to A6 receiver IF.

A6 Receiver IF

The A6 Receiver IF converts the 21.42 MHz 2nd IF from A4A2 to the final 3rd IF. The 3rd IF is then converted to a digital value in the A/D converter. The digital signal is routed to the DSP on the A1 CPU.

The A6 receiver IF consists of the following circuits (See Figure 11-12):

- Third Local Oscillator
- Third Converter
- Sample/Hold and A/D Converter
- Gains X, Y, and Z

Third Local Oscillator

The third local oscillator is a phase locked oscillator. The output signal is phase locked to the 40 kHz frequency of the divider output. The oscillator generates the 85.6 MHz signal. The signal divided by the 1/4 divider. The resulting 21.4 MHz signal is supplied to the third converter.

The oscillator contains an 85.6 MHz VCXO, a phase detector, a 1/2 divider, a mixer, and a 1/70 divider. See Figure 11-12. The VCXO frequency ($\mathbf{F_{vcxo}}$) is divided by 2 and mixed with the 40 MHz reference frequency in the mixer. The mixer then produces a shifted frequency ($\mathbf{F_{vcxo}}/2$ – 40 MHz). The mixer output is divided by 70 and then compared with the 40 kHz reference signal in the phase detector. Phase locking imposes the condition of 40 kHz = ($\mathbf{F_{vcxo}}/2$ – 40 MHz)/70. Therefore, the output frequency ($\mathbf{F_{vcxo}}$) is locked to 85.6 MHz (= (40 kHz × 70 + 40 MHz) x 2).

An unlock detector monitors the control voltage to the VCXO. When the control voltage is out of limits, the detector sends the status to the A1 CPU. Then the A1 CPU causes the message **CAUTION: PHASE LOCK LOOP UNLOCKED** to be displayed.

The VCXO is optimized by the "Third Local VCXO Adjustment."

Third Converter

In the third converter, the 21.42 MHz second IF is mixed with the 21.4 MHz third local signal and then converted to the final 20 kHz third IF.

The third converter is an image rejection mixer that rejects the 20 kHz signal converted from 21.38 MHz and 21.4 MHz. It also rejects errors caused by the 21.38 MHz component mixed into the second IF.

In the mixer, the 21.42 MHz second IF is divided into two paths (0° path and 90° path) and then mixed with the 90° phase different 21.4 MHz signals. Therefore, the 90° phase different 20 kHz signals are converted. The 90° path 20 kHz lags the 0° path 20 kHz by 90°s. Then the two phase shifters shift the 90° path 20 kHz forward by 90°. Therefore, the 90° path and the 0° path signals are in phase. Then the third IF signal is generated by adding the two 20 kHz signals that are in phase.

When 21.38 MHz signal is applied to the mixer. The 90° path mixer output 20 kHz forwards that of 0° path by 90°. Therefore, the 90° path phase sifter output 20 kHz forwards that of 0° path by 180°. These two signals are canceled by being added to each other.

Sample/Hold and A/D Converter

The 3rd IF is sampled and held in the Sample/Hold circuit. The hold signal is applied to the A/D converter through the A/D multiplexer and then converted to a digital value. The A/D multiplexer multiplexes the hold signal and the DC bus.

The DC bus is a single multiplexed line that networks 26 nodes within the HP 4286A. When the DC bus is connected to the A/D converter, the A/D converter is used to measure the voltage at a selected node within the HP 4286A. For more information about the DC bus measurement, see Chapter 10.

The analyzer has a 16 bit A/D converter capable of sampling at 100 ks/sec. In this application, it samples at the rate of 80 ks/sec. The sequencer consists of four GALs (gate array logic) ICs that are used as follows:

- Timing generator for the sample/hold the A/D converter.
- Timing generator/Gate shaper for the real time gated analysis.
- Timer driver/Input multiplexer driver/Frequency increment driver (controlling A5 FRAC N OSC).
- Decoder for the control signal from the A1 CPU.

Gains X, Y, and Z

The gains X (0 dB/6 dB/12 dB), Y (0 dB/6 dB/12 dB/18 dB), and Z (0 dB/2 dB/4 dB/18 dB) are variable amplifiers.

These amplifiers are used to optimize the IF gain (total gain through the 1st/2nd/3rd IF signal path) in order to use the A/D converter's widest possible dynamic range. The analyzer coarsely measures device impedance to determine the amplifiers' gains, then measures device impedance with optimum gain setting.

TEST HEAD THEORY

The test head receives the test signal from the source group and applies the test signal to the device under test (DUT). At the same time, the test head senses two signals that represent the voltage across the DUT and the current through the DUT, multiplexes the signals, and applies the signals to the receiver group.

Figure 11-7 is the simplified block diagram of the HP 4286A's impedance measurement.

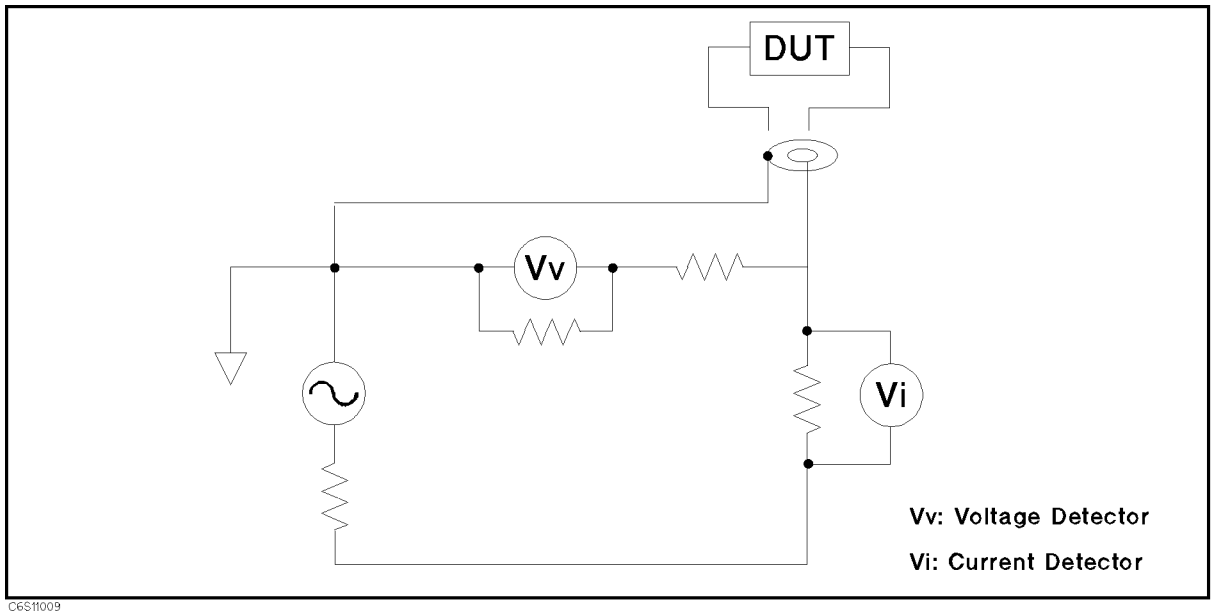


Figure 11-7. Simplified Impedance Measurement Block Diagram

Figure 11-2 is the test head block diagram. The test head consists of the following blocks:

- Transducer
- V/I Multiplexer
- Head Control

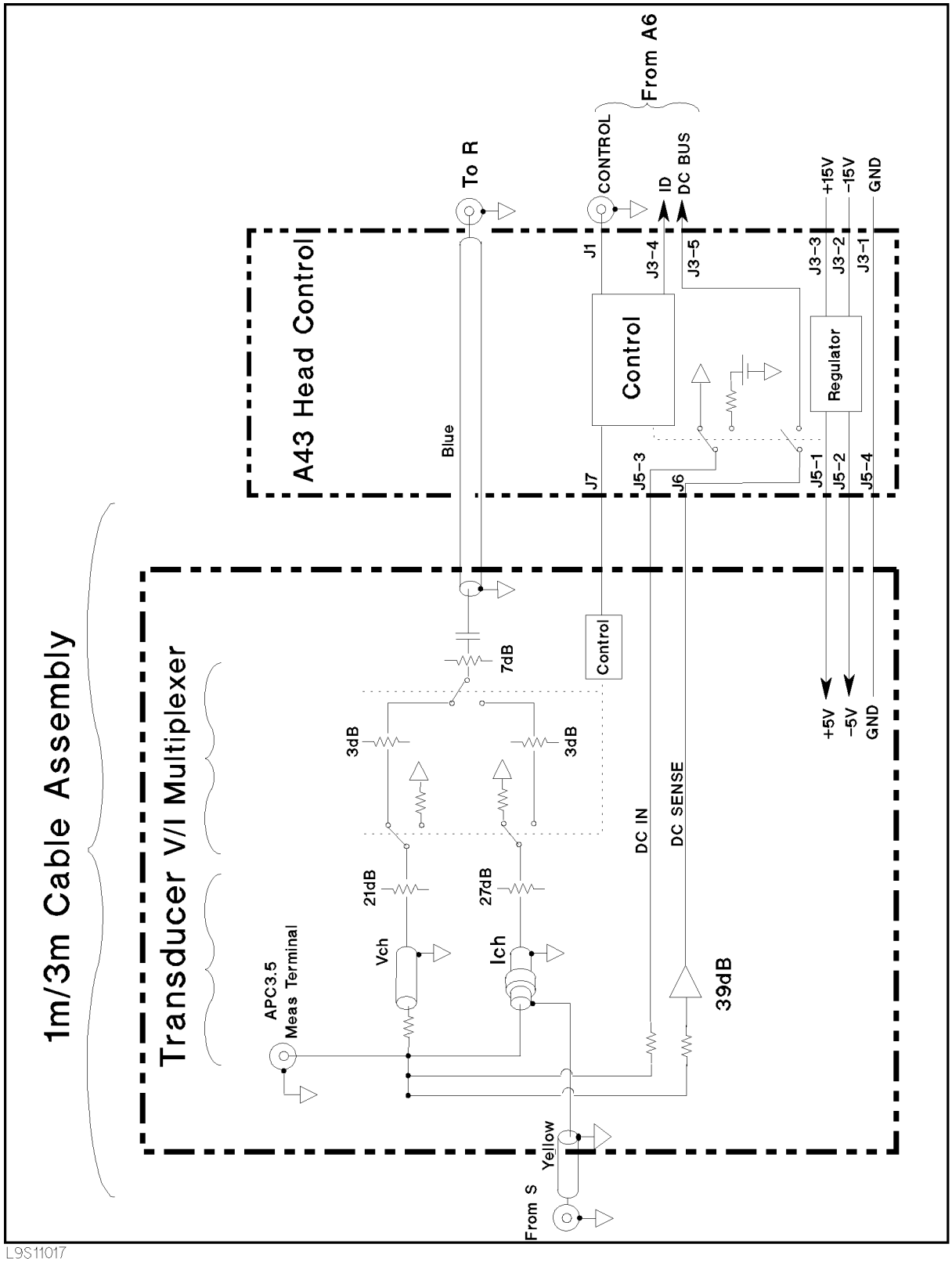


Figure 11-8. Test Head Block Diagram

Transducer

The transducer block senses the voltage across the DUT and the current through the DUT for the impedance measurement.

The transducer block also senses the DC voltage across the DUT for the contact check function.

V/I Multiplexer

The V/I multiplexer multiplexes the V and I signals from the test head. The multiplexer is a semiconductor switch.

A43 Head Control

The A43 head control receives the control data from the A6 receiver IF as serial data. It uses this data to control the V/I multiplexer and the swichs of the DC voltage source / DC voltage sensing line on the A43 head control.

The A43 head control receives the test head ID data and converts the data to serial data. It then forwards the data to the A6 receiver IF.

The A43 head control supplies the DC voltage for measuring the DC resistance of the DUT, which is used for the contact check function.

DC Resistance Measurement

The HP 4286A measures the DC resistance of the DUT when `RDC MEAS` is turned on. The DC voltage from the A43 head control is applied to the DUT, and the DC voltage across the DUT is monitored with the DC bus. Then the DC resistance is calculated from the monitored DC voltage.

The DC resistance measurement is effective after the calibration is performed at the measurement terminal.

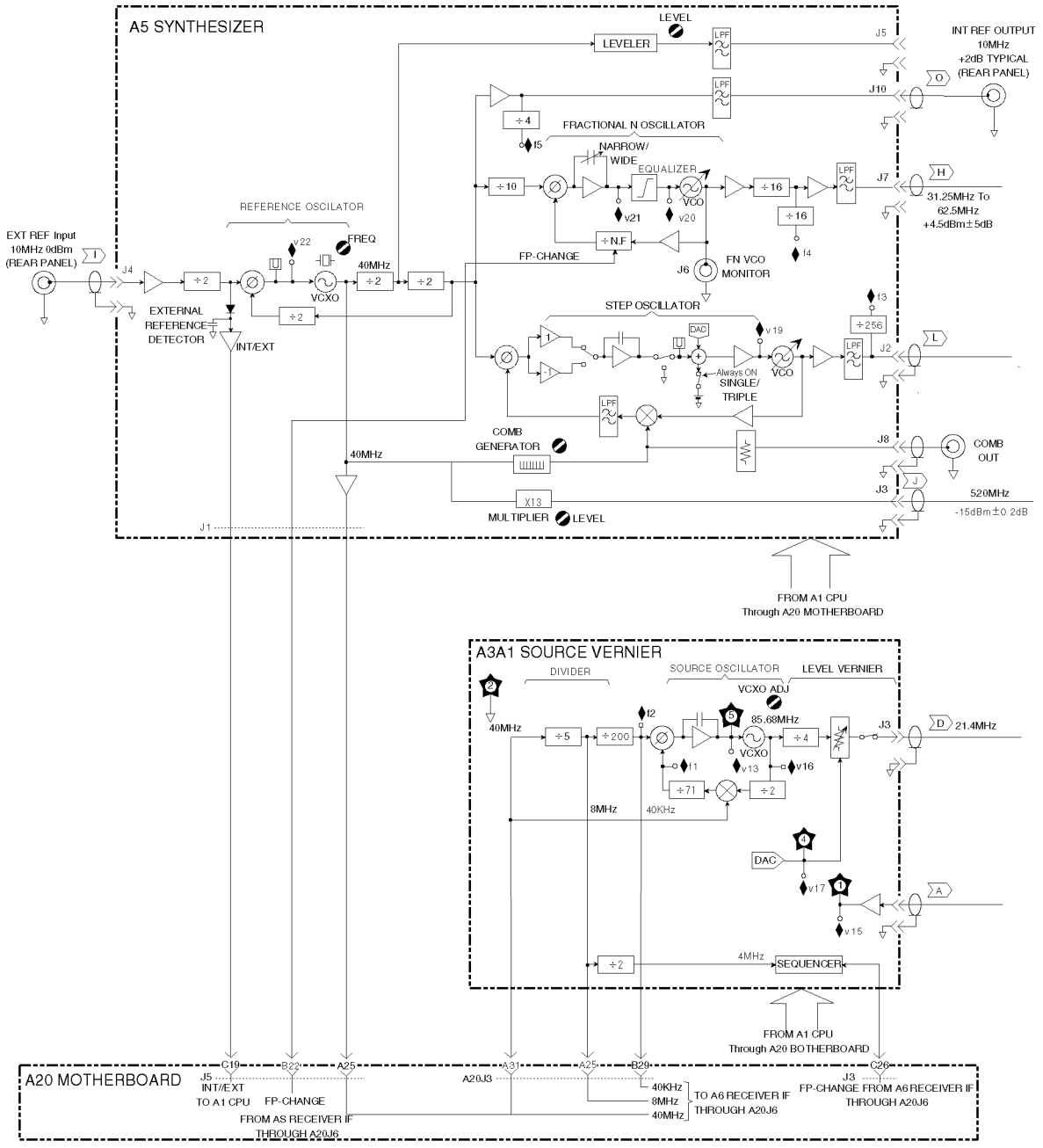


Figure 11-9. Source Group Block Diagram (1)

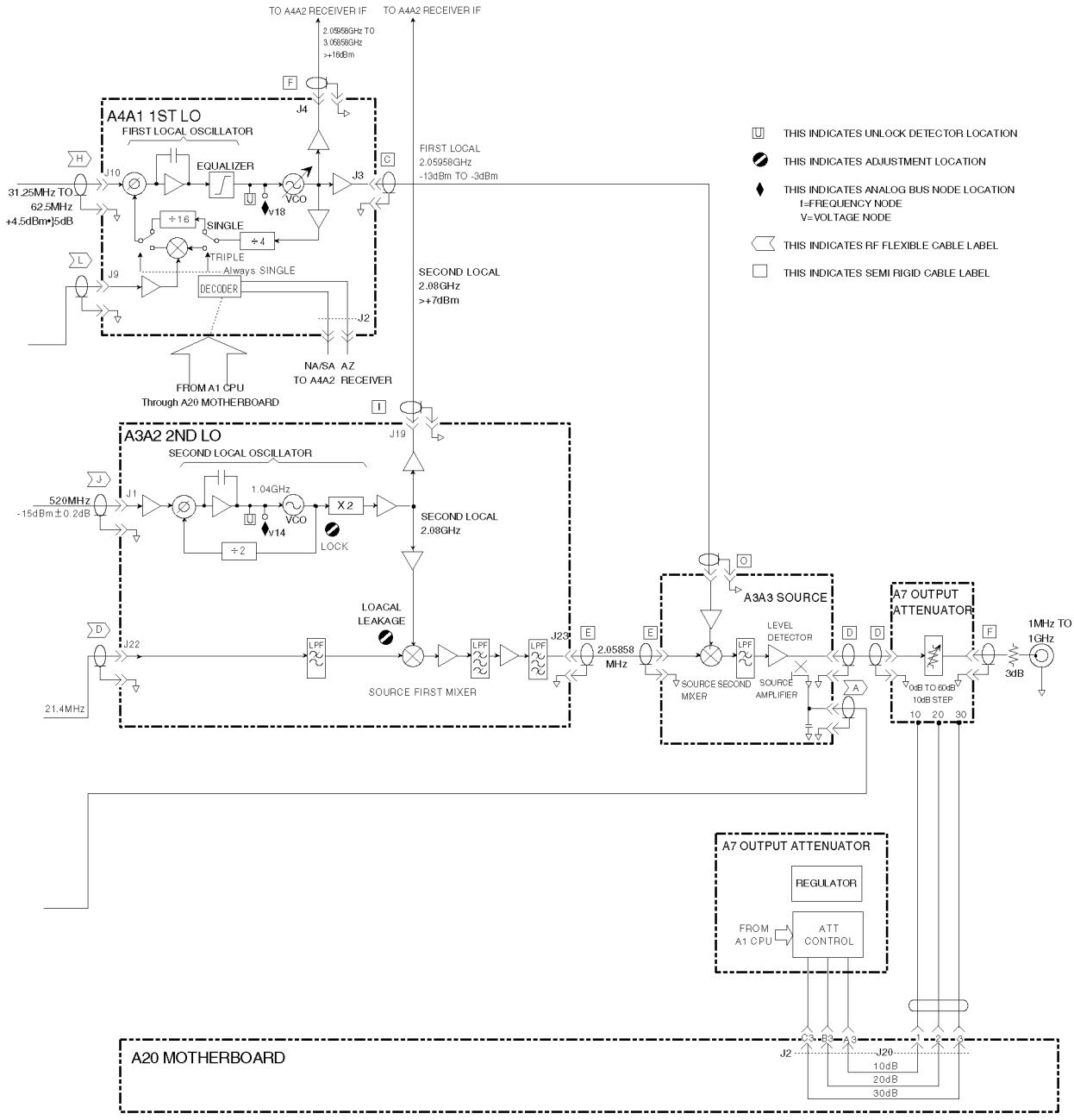


Figure 11-10. Source Group Block Diagram (2)

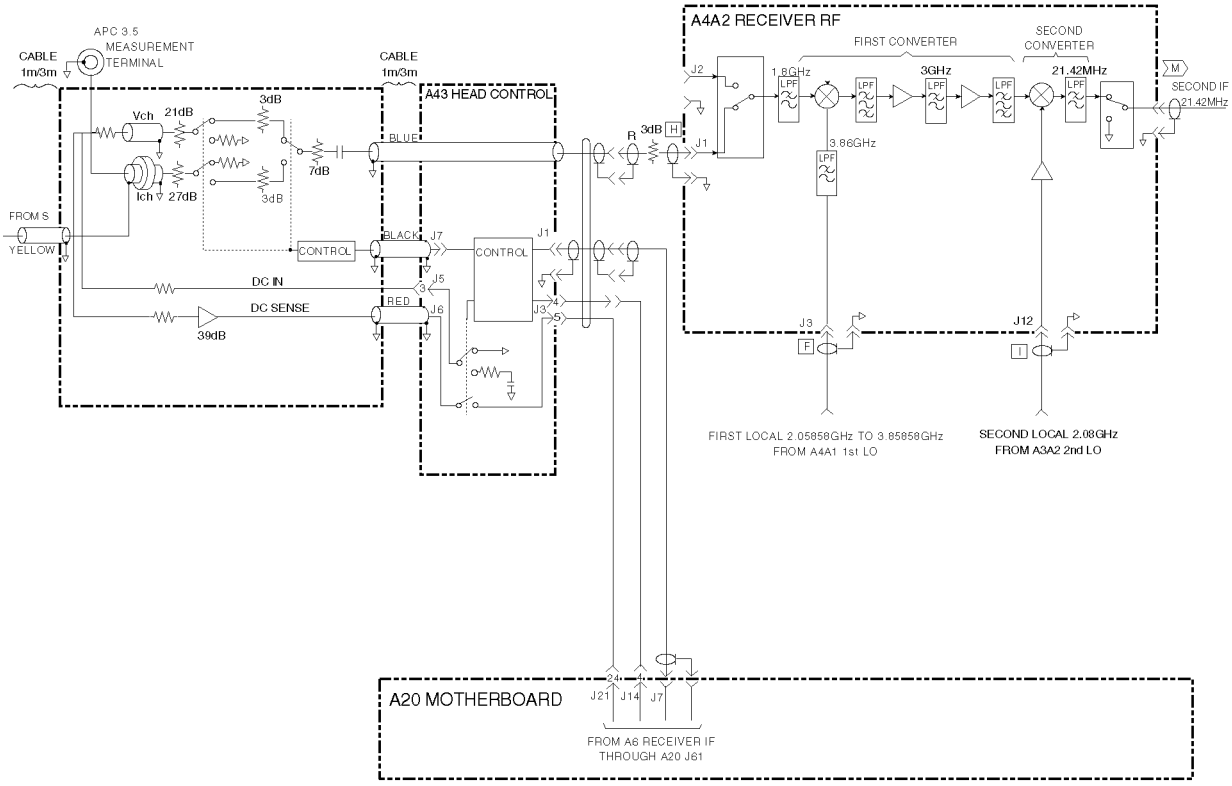


Figure 11-11. Receiver and Test Head Groups Block Diagram (1)

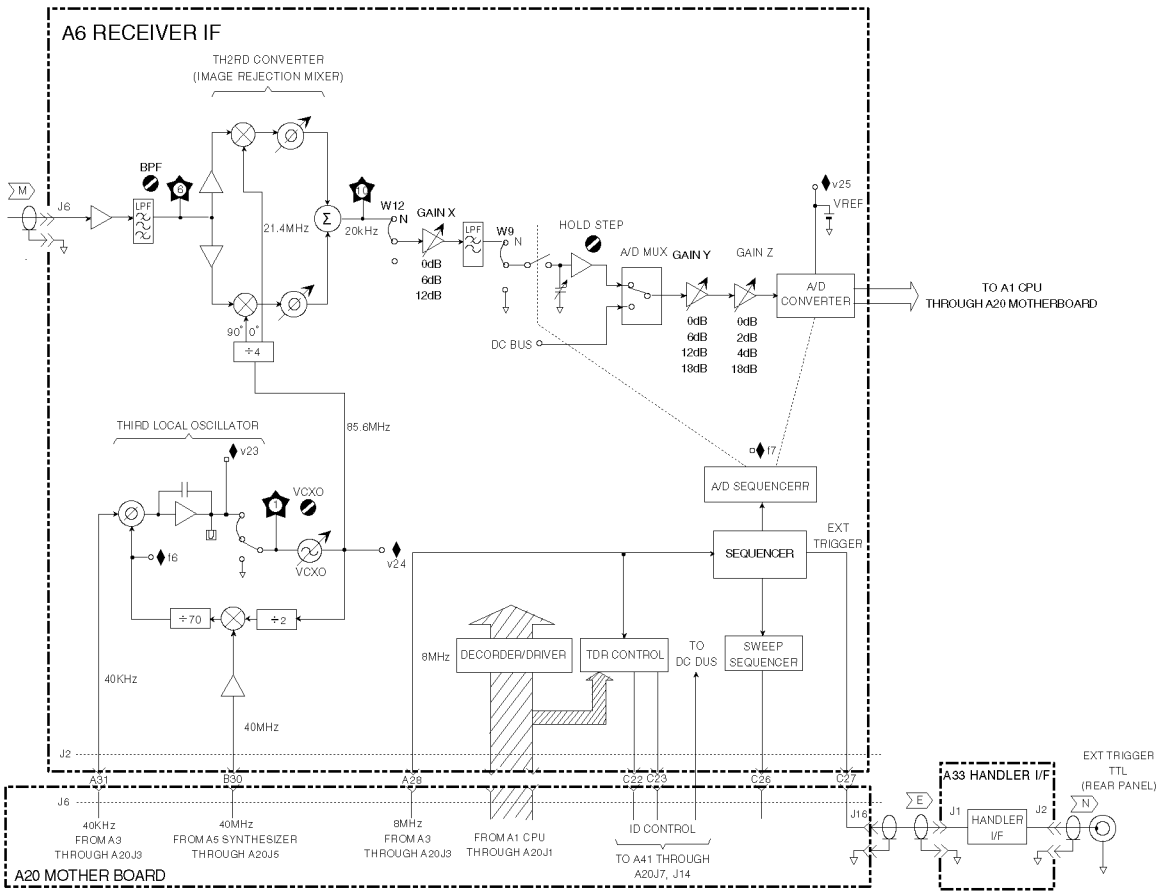


Figure 11-12. Receiver and Test Head Groups Block Diagram (2)

12

Replaceable Parts

INTRODUCTION

This chapter lists the HP 4286A's replaceable parts. How to order the parts is also described.

ORDERING INFORMATION

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with a check digit), indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of the order.

To order a part not listed in the replaceable parts table, include the instrument model number, the description and function of the part, and the quantity of parts required. Address the order to the nearest Hewlett-Packard office.

Direct Mail Order System

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are:

1. Direct ordering and shipment from the Hewlett-Packard Parts Center in Mountain View, California.
2. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local Hewlett-Packard office when the orders require billing and invoicing).
3. Prepaid transportation (there is a small handling charge for each order).
4. No invoices.

To provide these advantages, a check or money order must accompany each order.

Mail order forms and specific ordering information are available through your local Hewlett-Packard office, addresses and phone numbers are located at the back of this manual.

EXCHANGE ASSEMBLIES

Under the rebuilt-exchange assembly program, certain factory-repaired and tested assemblies are available on a trade-in basis. These assemblies are offered at lower cost than a new assembly while meeting all of the factory specifications required of a new assembly.

REPLACEABLE PARTS LIST

Replaceable parts tables list the following information for each part.

1 Hewlett-Packard part number.
2 Part number check digit (CD).
3 Part quantity as shown in the corresponding figure. There may or may not be more of the same part located elsewhere in the instrument.
4 Part description, using abbreviations (see Table 12-2).
5 A typical manufacturer of the part in a five-digit code (see Table 12-1).
6 The manufacturer's part number.

Table 12-1. Manufacturers Code List

Mfr #	Name	Location	Zipcode
00779	AMP INC	HARRISBURG PA US	17111
06369	HIROSE ELECTRIC CO	JP	
06691	HOUSE OF METRICS LTD	SPRING VALLEY NY US	10977
08747	KITAGAWA KOGYO	TOKYO JP	
09635	TAJIMI MUSEN	TOKYO JP	
10572	XICOR INC	MILPITAS CA	
12085	SCHLEGEL CORP	ROCHESTER NY US	14692
13160	TEAC OF AMERICA INC	MONTEBELLO CA US	90640
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA US	94304
28520	HEYCO MOLDED PRODUCTS	KENTWORTH NJ US	07033
73734	FEDERAL SCREW PRODUCTS CO	CHICAGO IL US	60618
76381	3M CO	ST PAUL MN US	55144
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF	ELGIN IL US	60126

Table 12-2. List of Abbreviations

A	: amperes	N/C	: normally closed
A.F.C.	: automatic frequency control	NE	: neon
AMPL	: amplifier	NI PL	: nickel plate
B.F.O	: beat frequency oscillator	N/O	: normally open
BE CU	: beryllium copper	NPO	: negative positive zero (zero temperature coefficient)
BH	: binder head	NPN	: negative-positive-negative
BP	: bandpass	NRFR	: not recommended for field replacement
BRS	: brass	NSR	: not separately replaceable
BWO	: backward wave oscillator	OBD	: order by description
CCW	: counter-clockwise	OH	: oval head
CER	: ceramic	OX	: oxide
CMO	: cabinet mount only	P	: peak
COEF	: coefficient	PC	: printed circuit
COM	: common	p	: pico
COMP	: composition	PH BRZ	: phosphor bronze
COMPL	: complete	PHL	: Philips
CONN	: connector	PIV	: peak inverse voltage
CP	: cadmium plate	PNP	: positive-negative-positive
CRT	: cathode-ray tube	P/O	: part of
CW	: clockwise	POLY	: polystyrene
DE PC	: deposited carbon	PORC	: porcelain
DR	: drive	POS	: position(s)
ELECT	: electrolytic	POT	: potentiometer
ENCAP	: encapsulated	PP	: peak to peak
EXT	: external	PT	: point
F	: farads	PWV	: peak working voltage
f	: femto	RECT	: rectifier
FH	: flat head	RF	: radio frequency
FIL H	: fillister head	RH	: round head or right hand
FXD	: fixed	RMO	: rack mount only
G	: giga	RMS	: root-mean square
GE	: germanium	RWV	: reverse working voltage
GL	: glass	S-B	: slow-blow
GRD	: ground(ed)	SCR	: screw
H	: henries	SE	: selenium
HEX	: hexagonal	SECT	: section(s)
HG	: mercury	SEMICON	: semiconductor
HR	: hour(s)	SI	: silicon
Hz	: hertz	SIL	: silver
IF	: intermediate freq.	SL	: slide
IMPG	: impregnated	SPG	: spring
INCD	: incandescent	SPL	: special
INCL	: include(s)	SST	: stainless steel
INS	: insulation(ed)	SR	: split ring
INT	: internal	STL	: steel
k	: kilo	TA	: tantalum
LH	: left hand	TD	: time delay
LIN	: linear taper	TGL	: toggle
LK WASH	: lock washer	THD	: thread
LOG	: logarithmic taper	TI	: titanium
LPF	: low pass filter	TOL	: tolerance
m	: milli	TRIM	: trimmer
M	: meg	TWT	: traveling wave tube
MET FLM	: metal film	μ	: micro
MET OX	: metallic oxide	VAR	: variable
MFR	: manufacturer	VDCW	: dc working volts
MINAT	: miniature	W/	: with
MOM	: momentary	W	: watts
MTG	: mounting	WIV	: working inverse voltage
MY	: “mylar”	WW	: wirewound
n	: nano	W/O	: without

Top View Assemblies

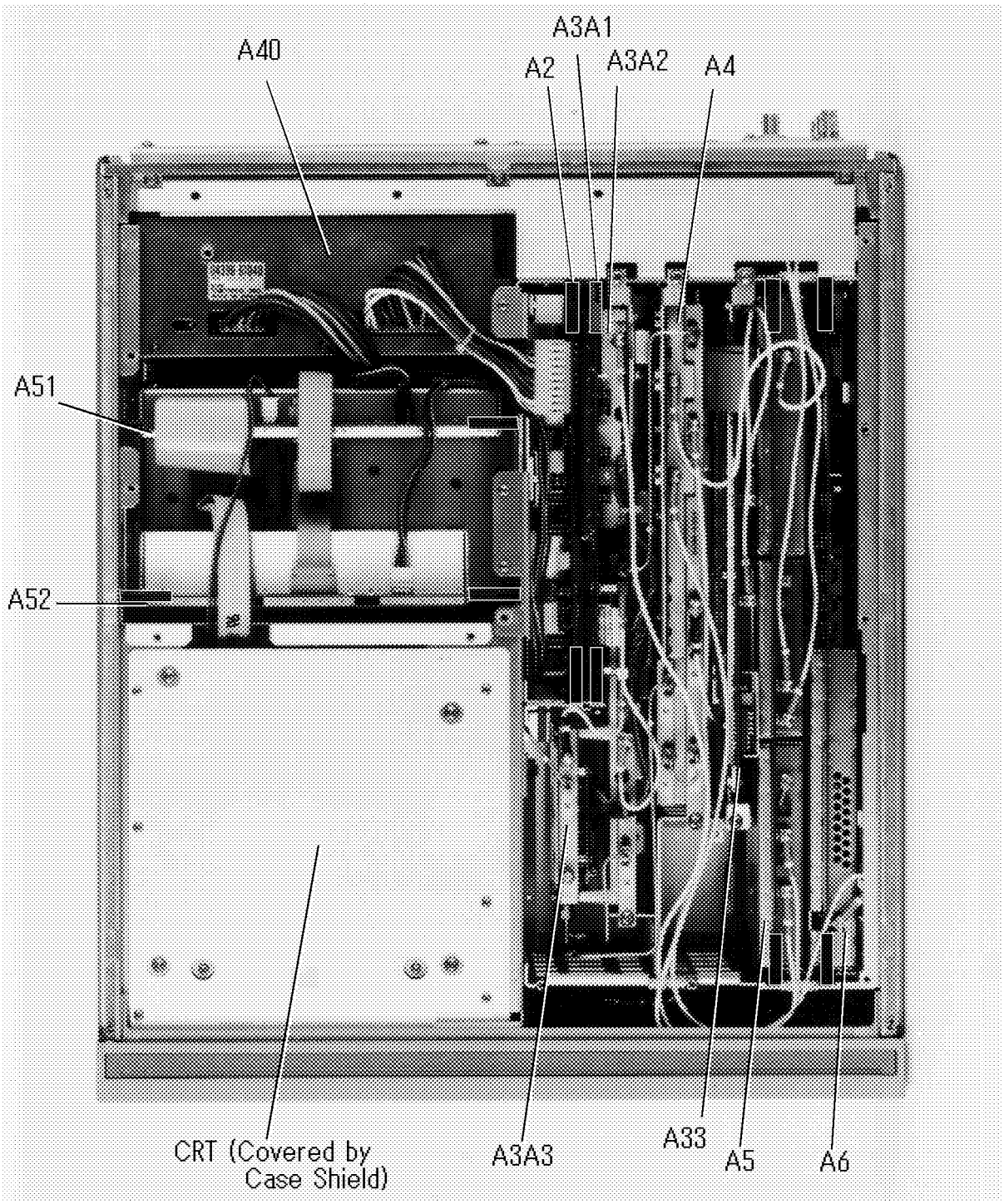


Figure 12-1. Top View 1 (Major Assemblies)

Table 12-3. Top View 1 (Major Assemblies)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
A2	04396-66502	6	1	Post Regulator	28480	04396-66502
A3A1	04291-66503	1	1	Source Vernier	28480	04291-66503
A3A2	04396-66513	9	1	Second Lo	28480	04396-66513
A3A2	04396-69513	5		Second Lo (rebuilt-exchange)	28480	04396-69513
A3A3	5086-7620	1	1	Source	28480	5086-7620
A3A3	5086-6620			Source (rebuilt-exchange)	28480	5086-6620
A4	04286-61004	3	1	First LO/Receiver RF	28480	04286-61004
A5	04396-66505	9	1	Synthesizer	28480	04396-66505
A5	04396-69505	5		Synthesizer (rebuilt-exchange)	28480	04396-69505
A6	04291-65506	4	1	Receiver IF	28480	04291-65506
A33	04286-66533	0	1	Handler I/F	28480	04286-66533
A40	04396-61040	7	1	Preregulator	28480	04396-66540
A40	04396-69040	3	1	Preregulator (rebuilt-exchange)	28480	04396-69540
A51	87510-66551	4	1	GSP	28480	08751-66551
A51	87510-69551	0		GSP (rebuilt-exchange)	28480	08751-69551
A52	04286-66552	3	1	DC-DC Converter	28480	04286-66552
CRT	See Table 12-14	7	1	CRT Assembly	28480	2090-0316

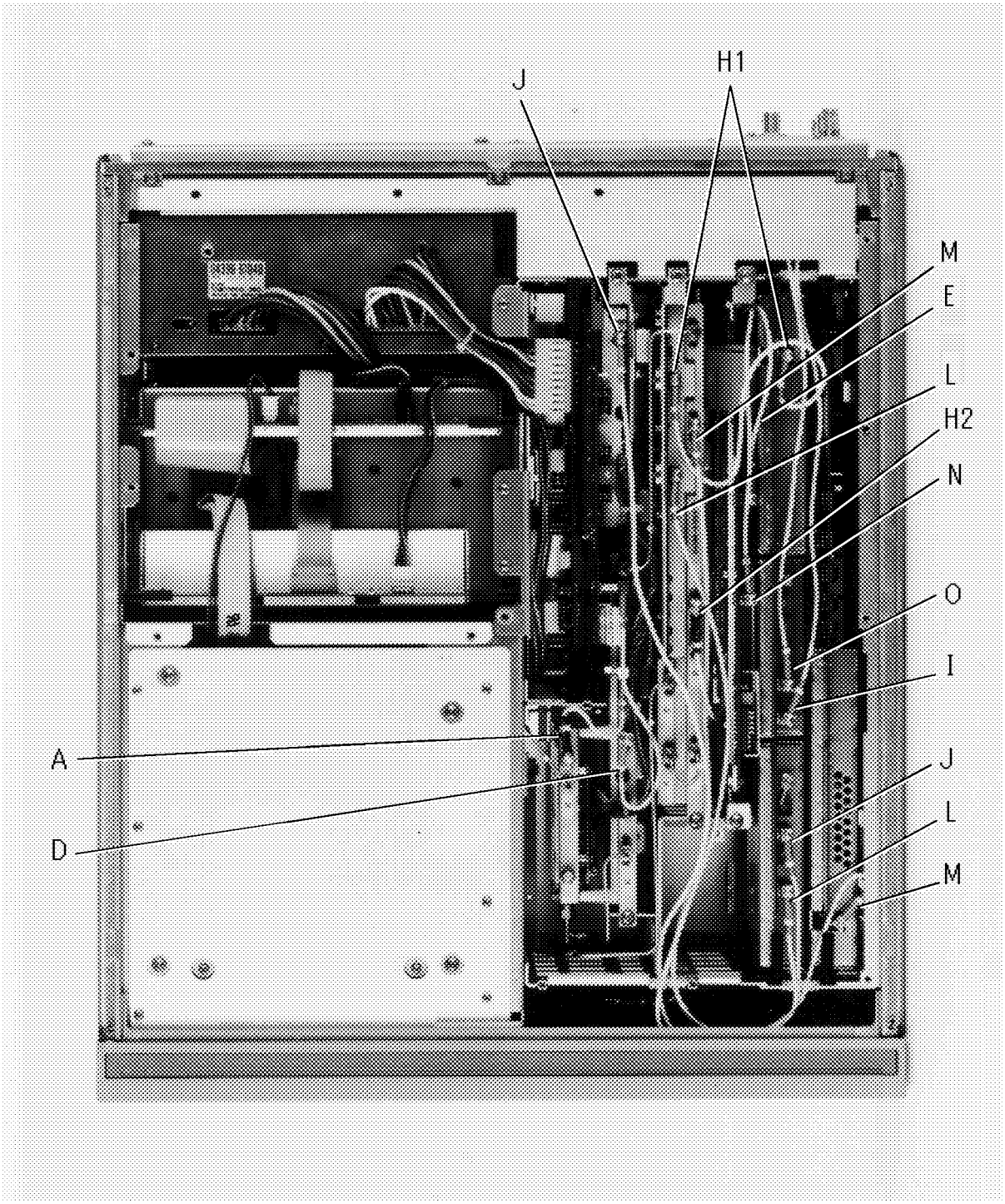


Figure 12-2. Top View 2 (RF Flexible Cables)

Note Alphabetic designators in Figure 12-2 show the cable markers.

Table 12-4. Top View 2 (RF Flexible Cables)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Connection	
A	04396-61621	0	1	RF Cable "A"	A3A1	A3A3
D	04396-61622	1	1	RF Cable "D"	A3A1	A3A2
E	04286-61605	7	1	RF Cable "E"	A20	A33
H_1	04396-61623	2	1	RF Cable "H"	A4	A5
H_2	04291-61615	6	1	RF Cable "H"	A4	Front "R"
I	04396-61634	5	1	RF Cable "I"	A5	Rear, EXT REF
J	04396-61625	4	1	RF Cable "J"	A3A2	A5
L	04396-61624	3	1	RF Cable "L"	A4	A5
M	04396-61626	5	1	RF Cable "M"	A4	A6
N	04286-61604	6	1	RF Cable "N"	A33	Rear, EXT TRIG
O	04396-61633	4	1	RF Cable "O"	A5	Rear, INT REF

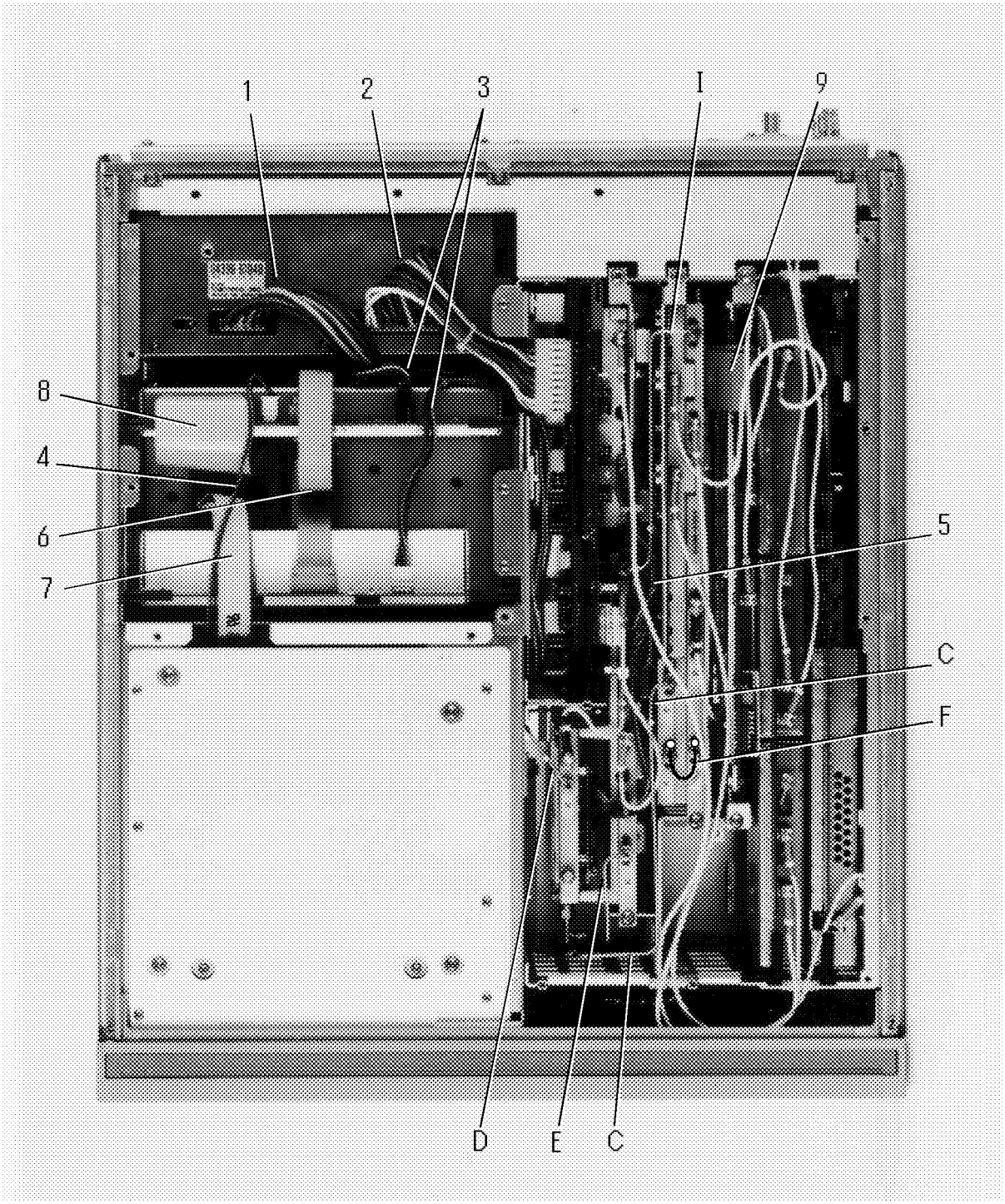


Figure 12-3. Top View 3 (RF Semi-rigid Cables, and Wires)

Note Alphabetic designators in Figure 12-3 show the cable markers.

Table 12-5. Top View 3 (RF Semi-rigid Cables, and Wires)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Connection	
C	04396-61603	8	1	RF Cable “C”	A3A3	A4
D	04291-61616	7	1	RF Cable “D”	A3A3	A7
E	04396-61605	0	1	RF Cable “E”	A3A2	A3A3
F	04396-61606	1	1	RF Cable “F”	A4	A4
I	04396-61609	4	1	RF Cable “I”	A3A2	A4
1	04396-61671	0	1	Wire	A1	A40
2	04396-61674	3	1	Wire	A2	A40
3	04286-61602	4	1	Wire	A2	A51, A52
4	04286-61606	8	1	Wire	A51	Front
5	04396-61673	2	1	Wire	A3A1	A3A2
6	04286-61603	5	1	Flat Cable	A51	A52
7	87510-61646	3	1	Flat Cable	A52	CRT
8	08751-61625	3	1	Flat Cable	A1	A51
9	04286-61601	3	1	Flat Cable	A31	A33

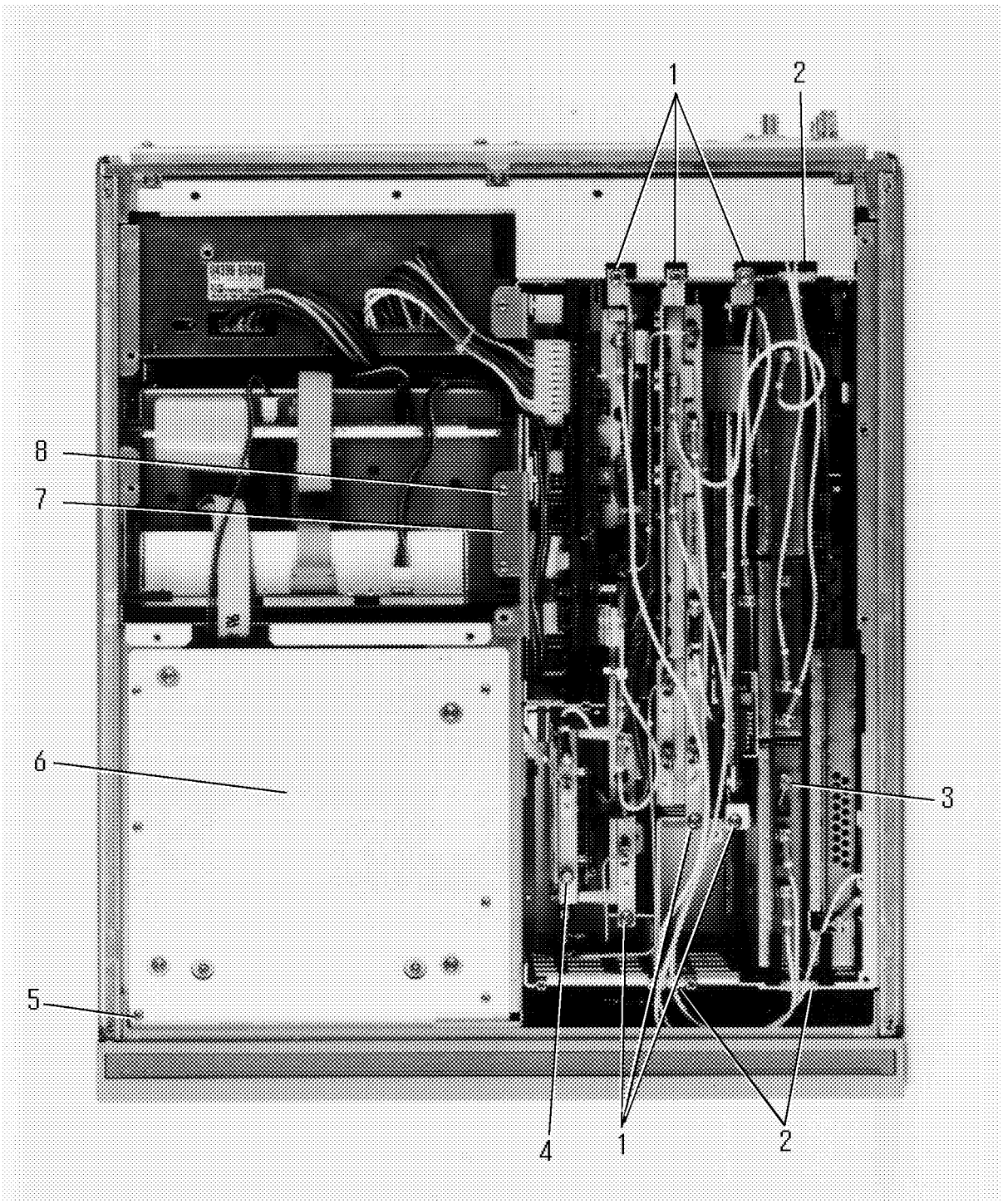


Figure 12-4. Top View 4 (Miscellaneous Parts)

Table 12-6. Top View 4 (Miscellaneous Parts)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	0515-2079	0	6	Screw M4 (for A3A2, A4, A33)	28480	0515-2079
2	1400-1048	9	3	Saddle Edge	28480	1400-1048
3	See Table 12-3			Termination (Part of A5)		
4	1810-0118	1	2	Termination SMA	28480	1810-0118
5	0515-1719	3	4	Screw M4	28480	0515-1719
6	See Table 12-20			CRT Plate Shield		
7	See Table 12-3			Heat Sink (Part of A2)		
8	0515-1550	0	3	Screw M3 (for A2)	28480	0515-1550
	0515-0889	6	8	Screw M3.5 (under Top Trim)	28480	0515-0889

Bottom View Assemblies

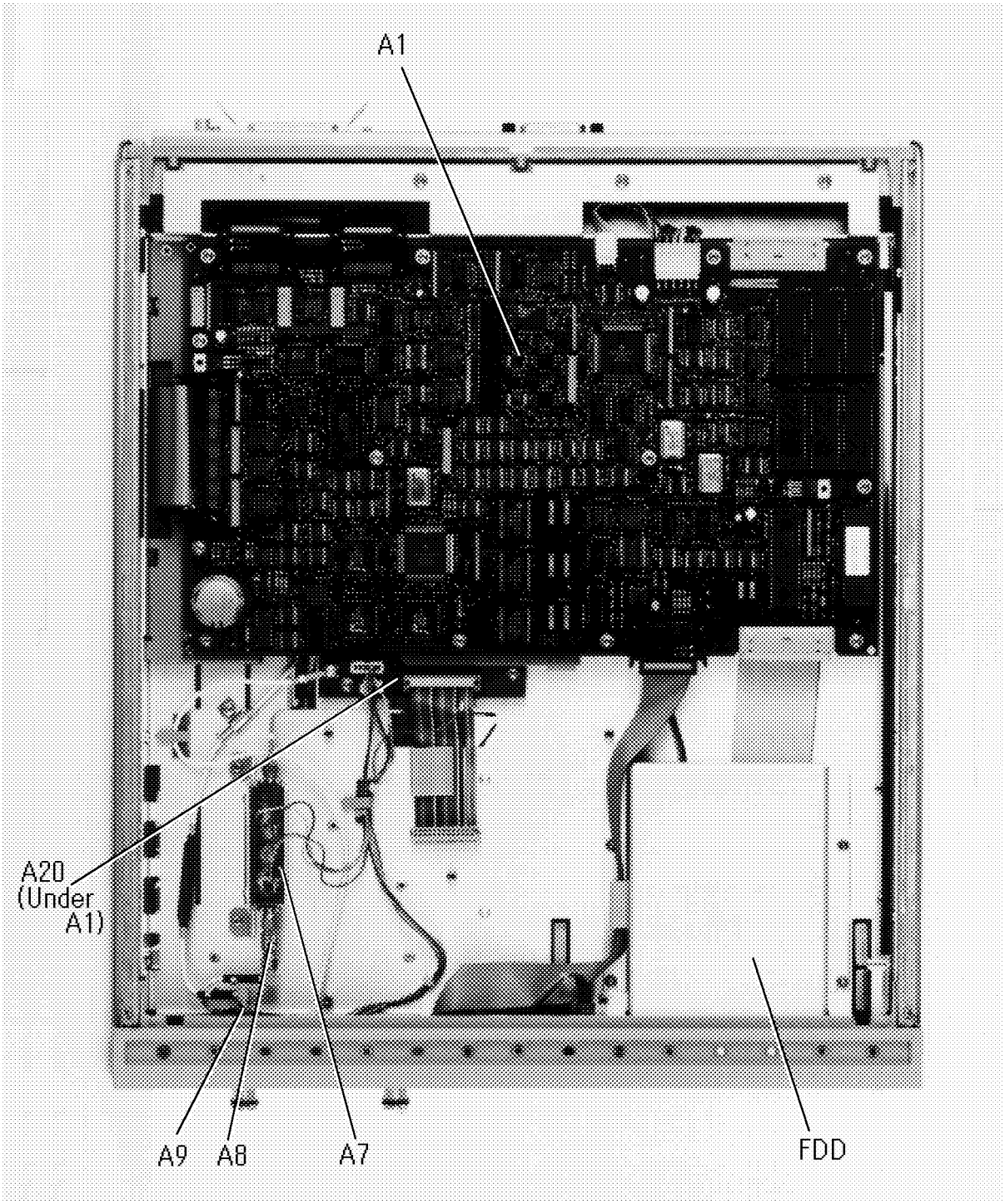


Figure 12-5. Bottom View 1 (Major Assemblies)

Table 12-7. Bottom View 1 (Major Assemblies)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
A1	04396-66501	5	1	CPU	28480	04396-66501
A1	04396-69501	1		CPU (rebuilt-exchange)	28480	04396-69501
A7	0955-0664	7	1	Output ATT	28480	0955-0664
A8	0955-0701	3	1	Output 3 dB ATT	28480	0955-0701
A9	0955-0701	3	1	Input 3 dB ATT	28480	0955-0701
A20	04291-66520	2	1	Motherboard	28480	04291-66520
FDD	0950-2267	0	1	Flexible Disk Drive	13160	FD-235HF-3428

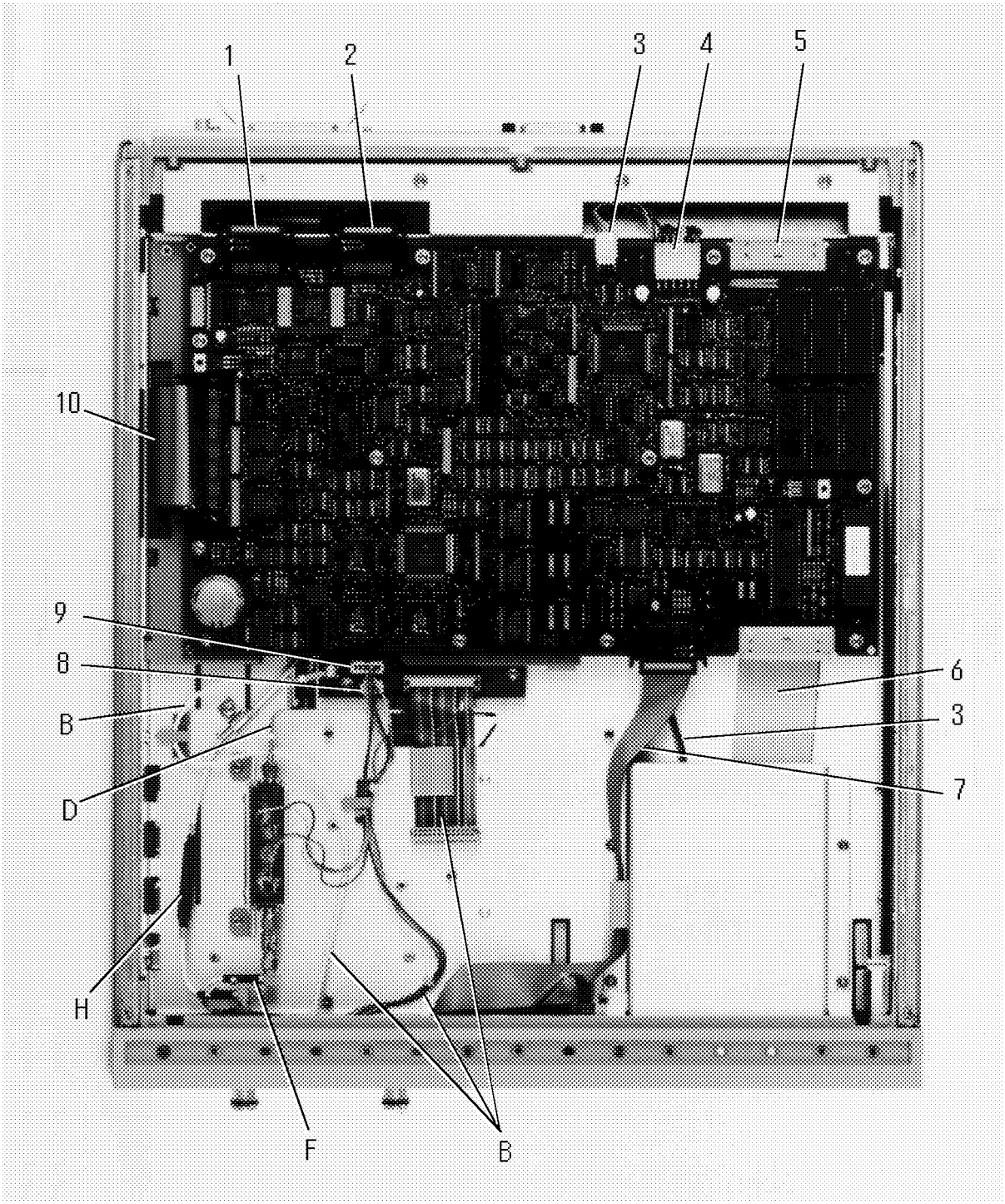


Figure 12-6. Bottom View 2 (RF Cables, and Wires)

Note Alphabetic designators in Figure 12-6 show the cable markers.

Table 12-8. Bottom View 2 (RF Cables, and Wires)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Connection	
B	04286-61001	9	1	Cable Assy "B"	Front	A20
D	See Table 12-5			RF Cable "D"	A3A3	A7
F	04291-61612	3	1	RF Cable "F"	Front "S"	A8
H	See Table 12-4			RF Cable "H"	Front "R"	A4
1	04396-61664	1	1	Flat Cable (Opt.1C2)	A1	A32
2	04396-61663	0	1	Flat Cable	A1	A31
3	04396-61672	1	1	Wire	A1	FDD
4	See Table 12-5			Wire	A1	A40
5	See Table 12-5			Flat Cable	A1	A51
6	04396-61651	6	1	Flat Cable	A1	FDD
7	04396-61662	9	1	Flat Cable	A1	A30
8	04291-61604	3	1	Wire	A7	A20
9	04286-61001	9	1	Cable Assy "B"	Front	A20
10	04396-61661	8	1	Flat Cable	A1	A20

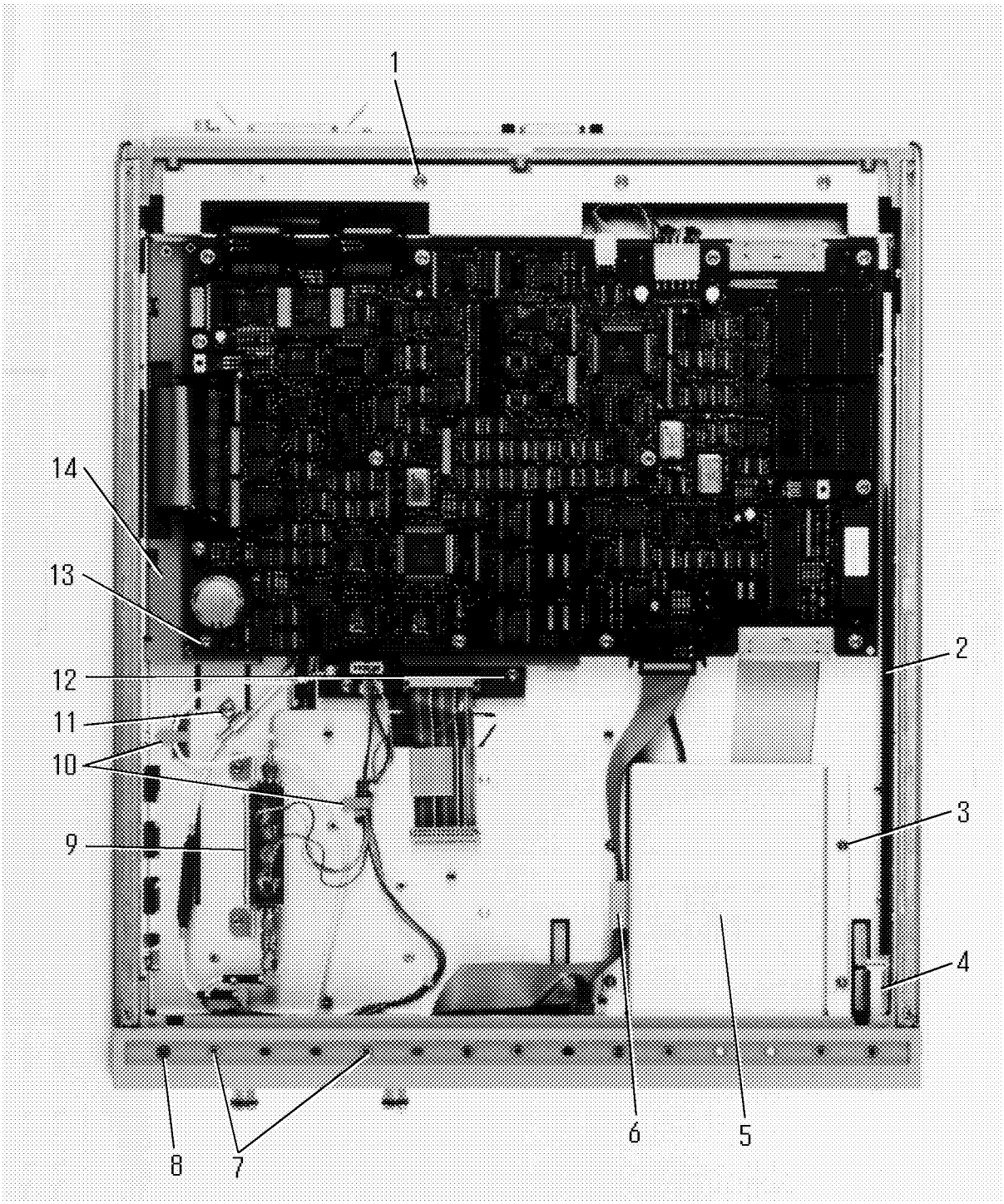


Figure 12-7. Bottom View 3 (Miscellaneous Parts)

Table 12-9. Bottom View 3 (Miscellaneous Parts)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	0515-1719	3	3	Screw M4	28480	0515-1719
2	04396-01202	7	1	Angle	28480	04396-01202
	1460-1573	1	1	Spring for Angle	28480	1460-1573
	0515-1550	0	1	Screw M3 (for Angle)	28480	0515-1550
	08751-23001	9	3	Guide	28480	08751-23001
	0515-0914	8	3	Screw M3 (for Guide)	28480	0515-0914
3	0535-0031	2	4	Nut M3	28480	0535-0031
4	5060-4076	1	1	Rod	28480	5060-4076
5	04396-01205	0	1	Holder	28480	04396-01205
	0515-0914	8	4	Screw M3 (for Holder)	28480	0515-0914
	04396-25004	7	1	Sponge (for Holder)	28480	04395-25004
6	1400-0611	0	1	Clamp Flat Cable	76381	3484-1000
7	0515-1011	8	2	Screw M3.5	28480	0515-1011
8	0515-0889	6	4	Screw M3.5	28480	0515-0889
9	04291-01231	6	1	Holder	28480	04291-01231
	0515-1550	0	4	Screw M3 (for Holder)	28480	0515-1550
10	1400-1334	6	2	Clamp Cable	28480	1400-1334
11	1400-0015	8	1	Clamp Cable	28480	1400-0015
	0515-2079	0	1	Screw M4	28480	0515-2079
12	0515-1550	0	14	Screw M3 (for A20)	28480	0515-1550
13	0515-1550	0	13	Screw M3 (for A1)	28480	0515-1550
14	04291-00110	8	1	Chassis	28480	04291-00110
	0515-0914	8	5	Screw M3 (for Chassis)	28480	0515-0914
	0403-0179	0	2	Bumper Foot	28480	0403-0719

Front Assembly Parts

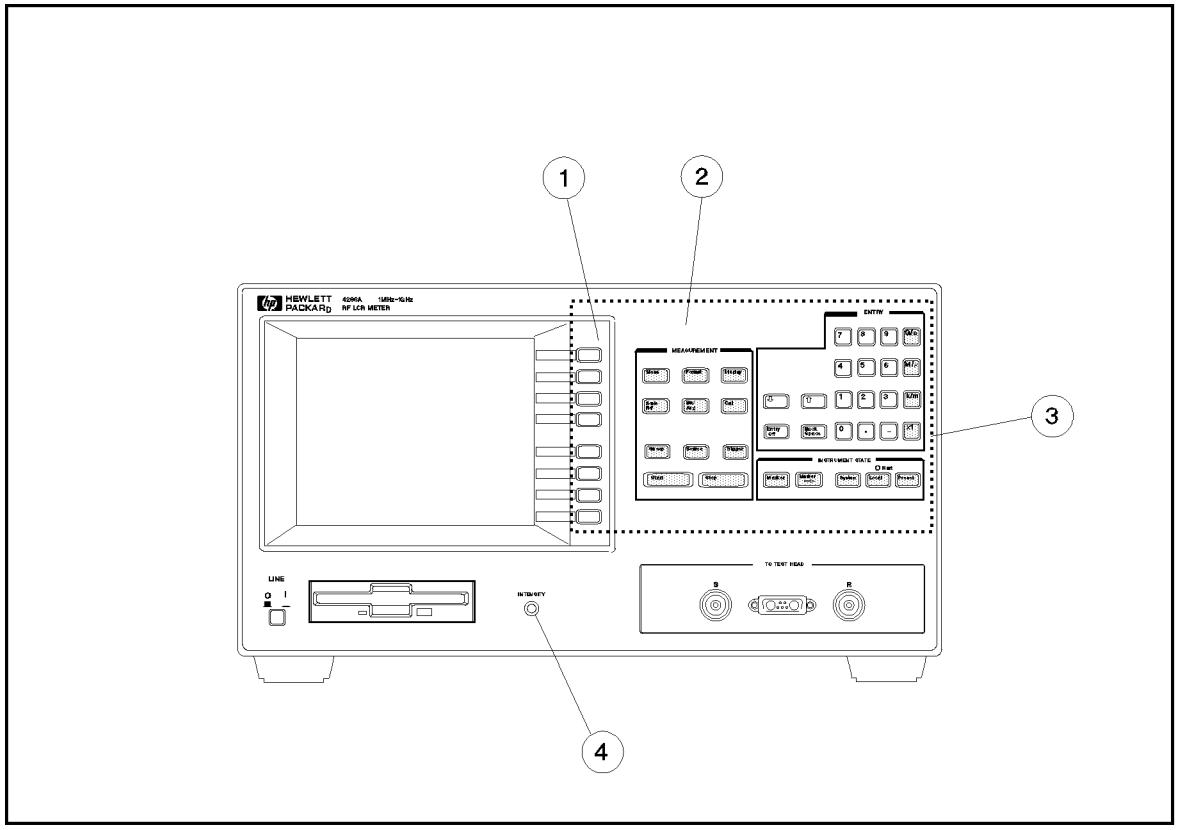


Figure 12-8. Front Assembly Parts 1 (Outside)

Table 12-10. Front Assembly Parts 1 (Outside)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	87510-40001	0	1	Bezel	28480	87510-40001
2	04286-00201	1	1	Panel Front	28480	04286-00201
	04286-00202	2	1	Panel Sub Front	28480	04286-00202
	04191-08000	0	1	Spring between Front Panel and Sub Panel	28480	04191-08000
3	04286-25001	1	1	Rubber Key	28480	04286-25001
4	See Table 12-5			Wire, A51 - Front		
	2190-0067	5	1	Washer	28480	2190-0067
	04145-24002	0	1	Nut	28480	04145-24002
	1400-1334	6	1	Clamp Cable	28480	1400-1334

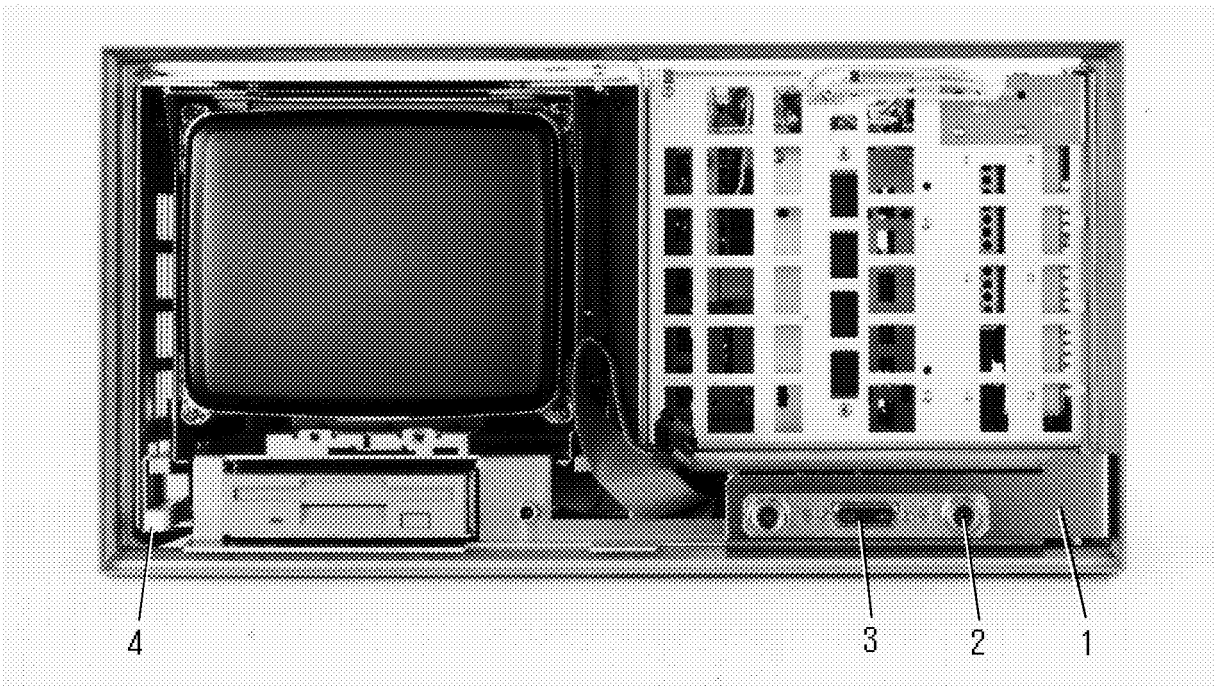


Figure 12-9. Front Assembly Parts 2 (Inside)

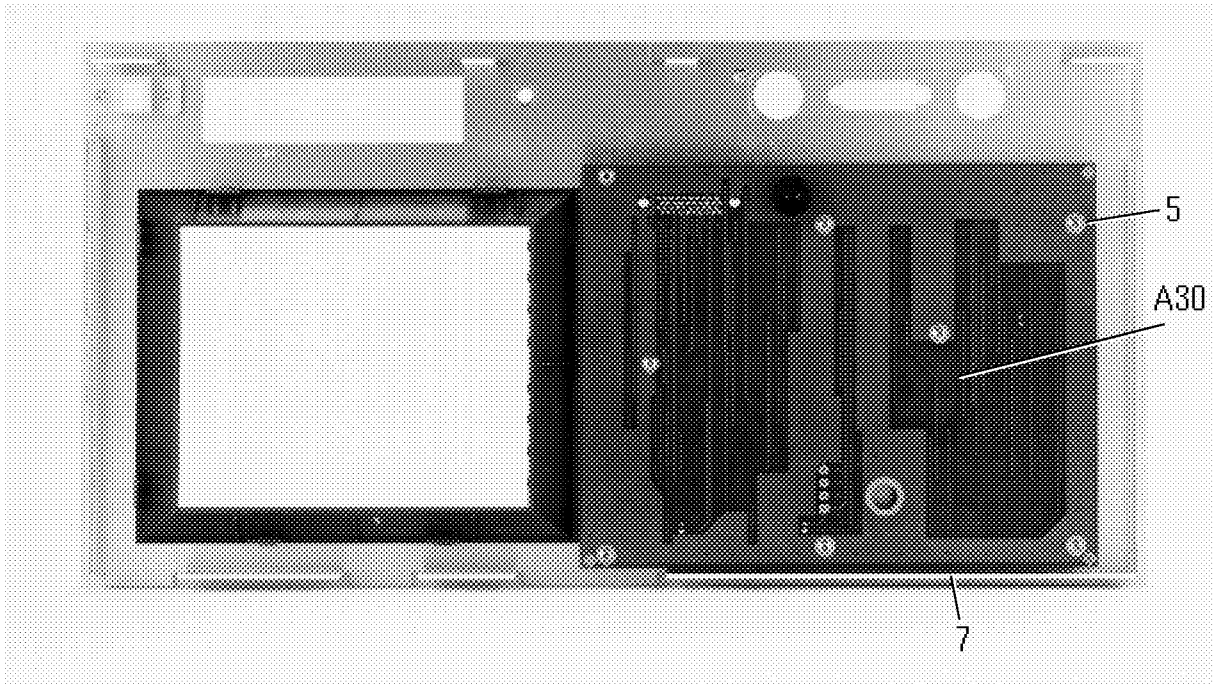


Figure 12-10. Front Assembly Parts 3 (Inside)

Table 12-11. Front Assembly Parts 2 (Inside)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
A30	04286-66530	7	1	Front Keyboard	28480	04286-66530
1	04286-01204	6	1	Angle	28480	04286-01204
2	1250-2205	3	2	Connector N Type	28480	1250-2205
	2190-0054	9	2	Washer (for Connector)	78189	1924-12
3[1]	04286-61001	9	1	Cable Assy "B"	28480	04286-61001
	04291-24002	7	2	Stud (for connector)	28480	04291-24002
	0535-0031	2	2	Nut (for connector)	28480	0535-0031
4[2]	5060-4076	1	1	Rod	28480	5060-4076
5	0515-1550	0	8	Screw M3 (for A30)	28480	0515-1550
6	04286-40001	6	1	Guide	28480	04286-40001

1 See Table 12-8

2 See Table 12-9

Rear Assembly Parts

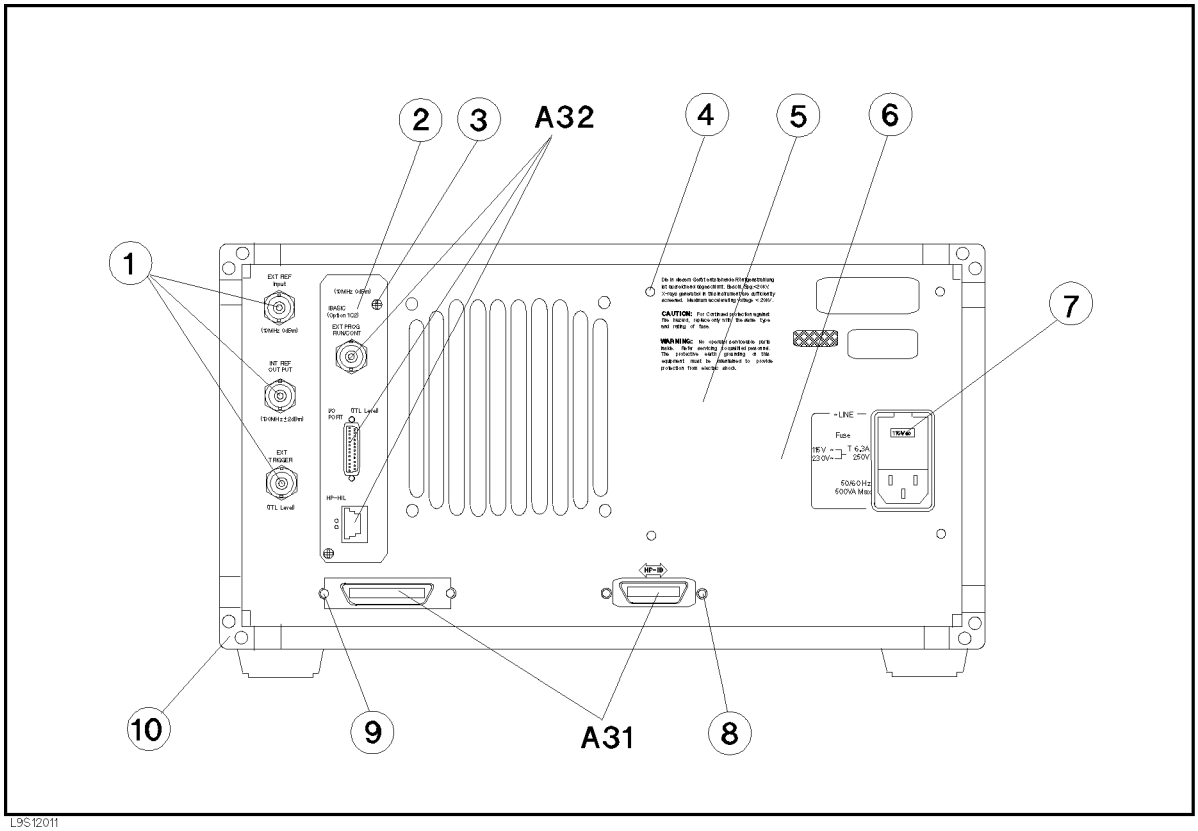


Figure 12-11. Rear Assembly Parts 1 (Outside)

Table 12-12. Rear Assembly Parts 1 (Outside)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
A31	04286-66531	8	1	I/F Connector Board	28480	04286-66531
A32	04396-66532	2	1	IBASIC I/F (Opt.1C2)	28480	04396-66532
	04396-24006	7	1	Spacer (for Connector)	28480	04396-24006
	2190-0054	9	1	Washer (for Connector)	78189	1924-12
	2950-0054	1	1	Nut (for Connector)	28480	2950-0054
	1251-5436	0	2	Screw (for Connector)	00779	205817-1
1	1250-0252	6	3	Connector BNC	28480	1250-0252
	2190-0102	8	3	Washer (for Connector)	78189	1922-01
	2950-0035	8	3	Nut (for Connector)	28480	2950-0035
2	04396-00210	5	1	Plate (Std.)	28480	04396-00210
	04396-00211	6	1	Plate (Opt.1C2)	28480	04396-00211
3	0515-1550	0	2	Screw M3	28480	0515-1550
4	0515-2079	0	4	Screw M4	28480	0515-2079
5	5080-3925	9	1	Label Opt.1C2	28480	5080-3925
6	04286-00203	3	1	Panel Rear	28480	04286-00203
	0363-0125	0	30cm	Gasket	28480	0363-0125
7	2110-0917	5	1	Fuse	28480	2110-0917
8	0380-0644	4	2	Standoff	28480	0380-0644
	2190-0577	9	1	Washer (for Standoff)	28480	2190-0577
9	0515-1550	0	2	Screw M3 (for A31)	28480	0515-1550
10	5041-8821	2	4	Stand Off	28520	5041-8821
	0515-1232	5	4	Screw M3	28480	0515-1232

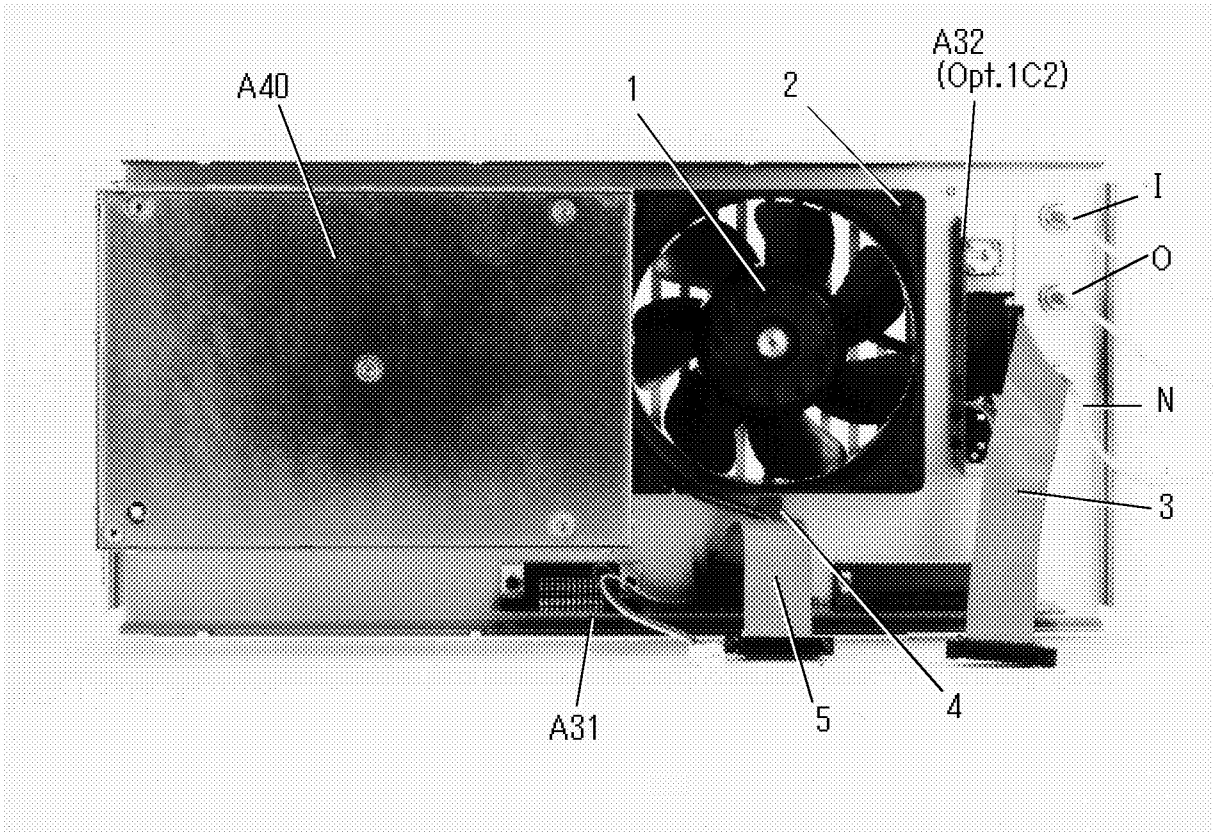


Figure 12-12. Rear Assembly Parts 2 (Inside)

Note Alphabetic designators in Figure 12-12 show the cable markers.

Table 12-13. Rear Assembly Parts 2 (Inside)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
A31	See Table 12-12			I/F Connector Board		
A32	See Table 12-12			IBASIC I/F (Opt.1C2)		
A40	See Table 12-3			Power Supply		
1	04396-61001	0	1	Fan Assembly	28480	04396-61001
2	3050-0893	9	4	Washer Flat	28480	3050-0893
	2190-0586	2	4	Washer Spring	06691	A2WASPSR 0158
	0515-1598	6	4	Screw M4	28480	0515-1598
3	See Table 12-8			Flat Cable (A32 to A1)		
4	1400-1334	6	1	Clamp Cable	28480	1400-1334
5	See Table 12-8			Flat Cable (A31 to A1)		
I	See Table 12-4			RF Cable “I”		
N	See Table 12-4			RF Cable “N”		
O	See Table 12-4			RF Cable “O”		

CRT Assembly

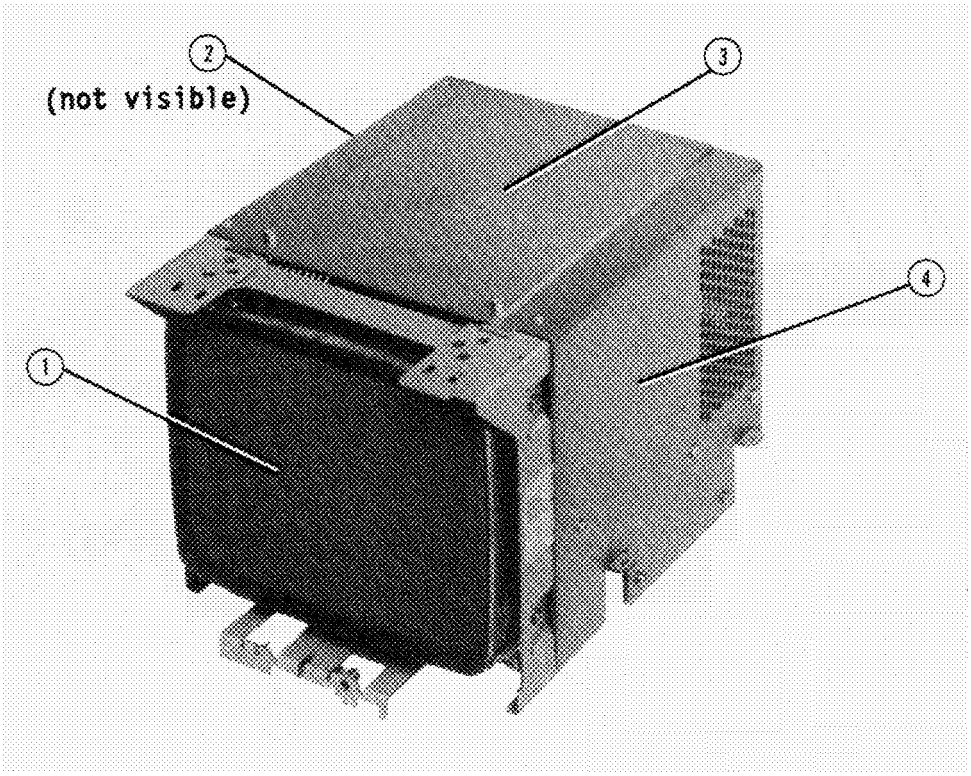


Figure 12-13. CRT Assembly

Table 12-14. CRT Assembly Parts

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	87510-65003	4	1	CRT	28480	87510-65003
2	87510-00622	7	1	Angle Left	28480	87510-00622
	0515-2055	2	3	Screw M3	28480	0515-2055
3	87510-00620	5	1	Cover Top	28480	87510-00620
	0515-1550	0	6	Screw M3	28480	0515-1550
4	87510-00621	6	1	Angle Right	28480	87510-00621
	0515-2055	2	3	Screw M3	28480	0515-2055
	See Table 12-5			Flatcable, CRT-A52		

Test Head Parts

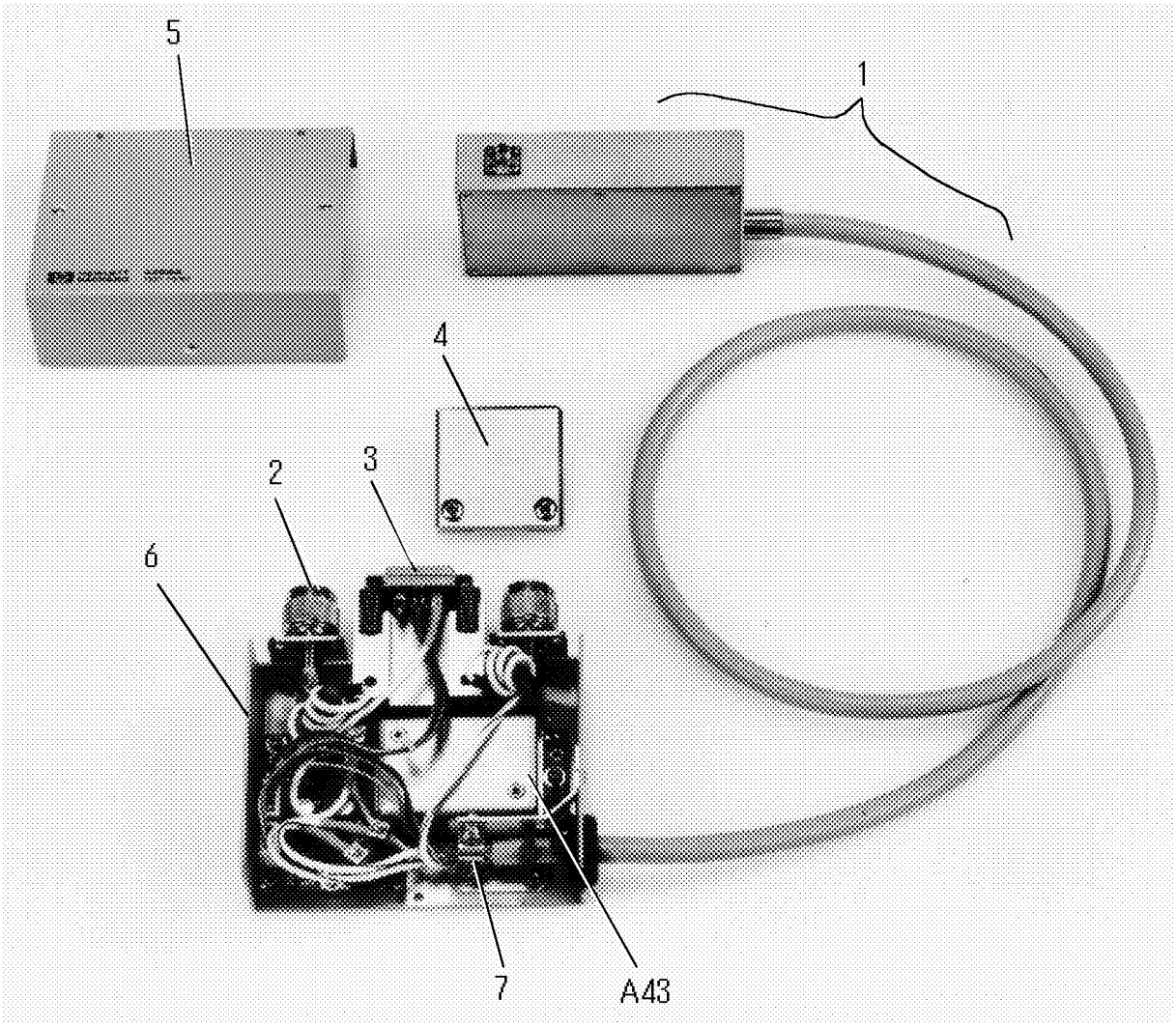


Figure 12-14. Test Head Parts

Table 12-15. Test Head Parts

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
	04286-60131[1]	2	1	Test Head Assy, Right Angle 1m	28480	04286-60131
	04286-60132[2]	3	1	Test Head Assy, Right Angle 3m	28480	04286-60132
	04286-60121[3]	0	1	Test Head Assy, Straight Angle 1m	28480	04286-60121
	04286-60122[4]	1	1	Test Head Assy, Straight Angle 3m	28480	04286-60122
1	04286-65031[1]	1	1	Cable Assy, Right Angle 1m	28480	04286-65031
	04286-65032[2]	2	1	Cable Assy, Right Angle 3m	28480	04286-65032
	04286-65021[3]	9	1	Cable Assy, Straight Angle 1m	28480	04286-65021
	04286-65022[4]	0	1	Cable Assy, Straight Angle 3m	28480	04286-65022
	1400-0493	6	2	Cable Tie	06383	PLT 1.5I-M8
2	1250-2468	0	2	Connector N(m)-SMA(f)	28480	1250-2468
	0515-0907	9	8	Screw M3L8 (for Connector)	28480	0515-0907
3	04286-61031	3	1	Connector Assy	28480	04286-61031
	1460-2369	5	2	Spring	28480	1460-2369
4	04286-20031	7	2	Connector Cover	28480	04286-20031
	0515-1718	2	2	Screw (for Connector Cover)	28480	0515-1718
5	04286-04031	3	1	Cover Top	28480	04286-04031
6	04286-04032	4	1	Cover Bottom	28480	04286-04032
7	1400-0015	8	1	Clamp Cable	28480	1400-0015
	0515-2079	0	1	Screw (for Clamp Cable)	28480	0515-2079
A43	04286-66543	2	1	Head Control Board	28480	04286-66543
	0515-1550	0	3	Screw (for A43)	28480	0515-1550

1 For standard type

2 For option 032

3 For option 021

4 For option 022

Note

"Cable Assy" designated ① in Figure 12-14 includes the APC3.5 measurement terminal block (end of the test head) and the 1m/3m cable (coaxial cables connected to S, R, A43J6 and A43J7, and the wire connected to A43J5).

"Connector Assy" designated ③ in Figure 12-14 includes the coaxial cable connected to A43J1 and the wire connected to A43J3.

Miscellaneous Parts

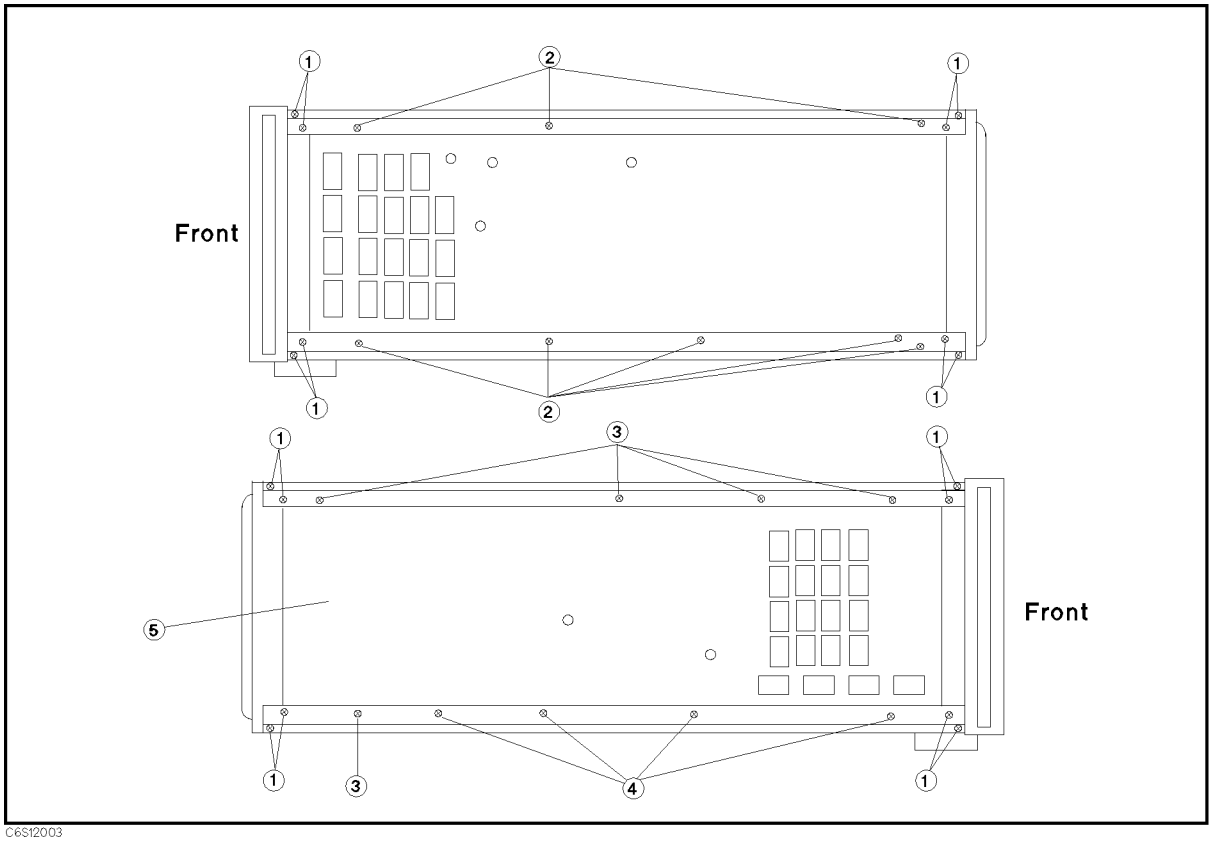


Figure 12-15. Miscellaneous Parts 1 (Side Views)

Table 12-16. Miscellaneous Parts 1 (Side Viwes)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	0515-1668	1	16	Screw	28480	0515-1668
2	0515-1719	3	8	Screw M4	28480	0515-1719
3	0515-2079	0	5	Screw M4	28480	0515-2079
4	0515-1718	2	4	Screw M4	28480	0515-1718
5	04286-60001	5	1	Chassis	28480	04286-60001

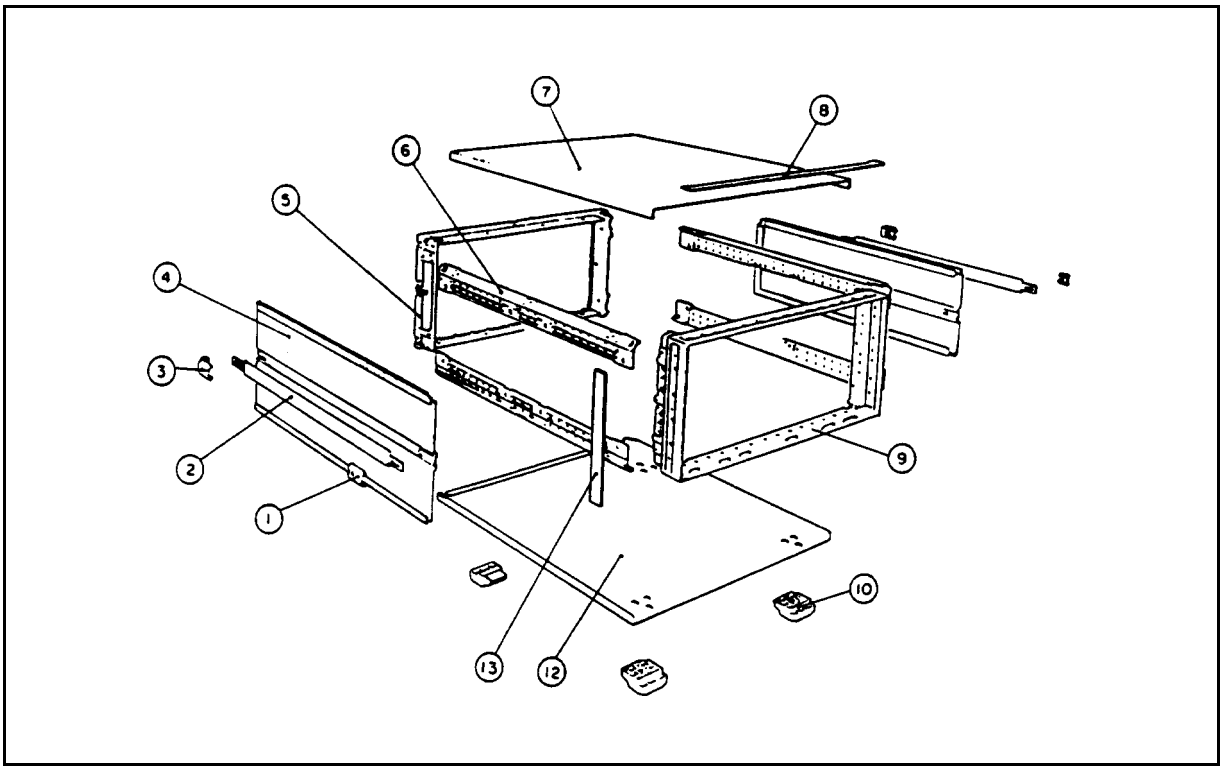


Figure 12-16. Misscellaneous Parts 2 (Chassis)

Table 12-17. Misscellaneous Parts 2 (Chassis)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	5041-8819	8	2	Cap-Front	28480	5041-8819
	0515-1132	4	2	Screw M5	28480	0515-1132
2	5062-3704	4	2	Strap Handle	28480	5062-3704
3	5041-8820	1	2	Cap-Rear	28480	5041-8820
	0515-1132	4	2	Screw M5	28480	0515-1132
4	5062-3847	6	2	Side Cover	28480	5062-3847
5	5021-5808	7	1	Rear Frame	28480	5021-5808
6	5021-5837	2	4	Corner Strut	28480	5021-5837
7	5062-3735	1	1	Top Cover	28480	5062-3735
8	5041-8802	9	1	Top Trim	28480	5041-8802
9	5021-8407	8	1	Front Frame	28480	5021-8407
10	5041-8801	8	4	Foot	28480	5041-8801
	1460-1345	5	2	Tilt Stand	28480	1460-1345
12	5062-3747	5	1	Bottom Cover	28480	5062-3747
13	5001-0541	3	2	Side Trim	28480	5001-0541

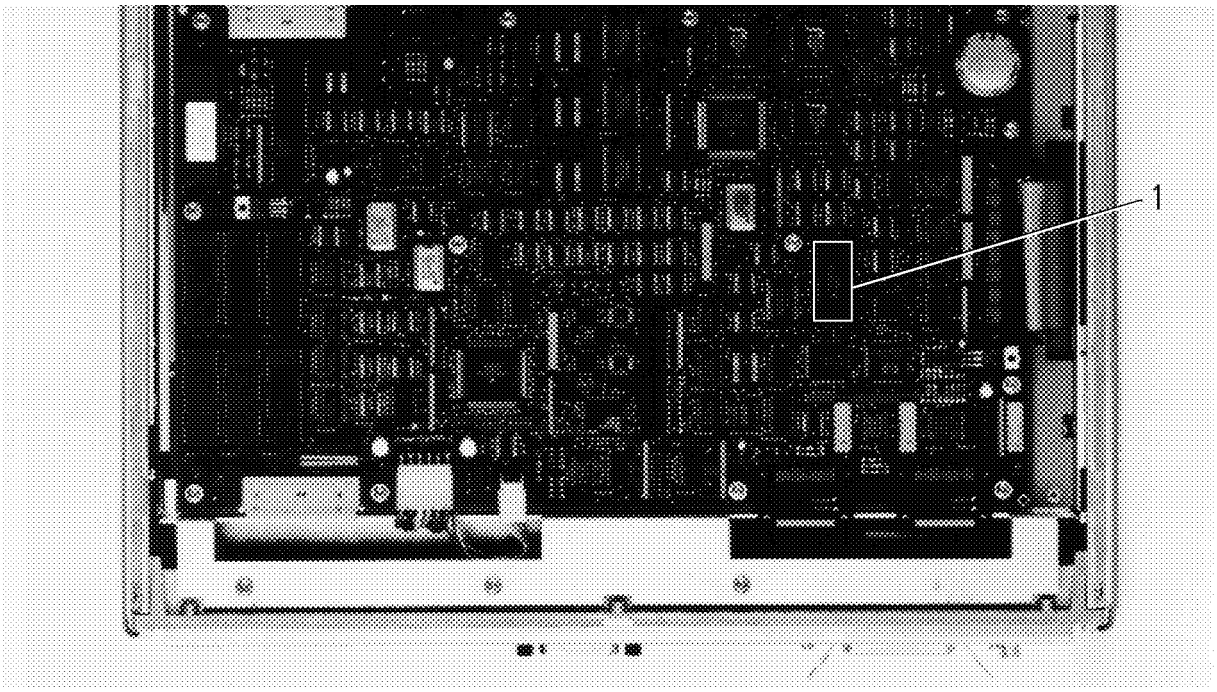


Figure 12-17. Miscellaneous Parts 4 (On A1)

Table 12-18. Miscellaneous Parts 4 (On A1)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	1818-5146	1	1	EEPROM[1]	10572	X28C64P-20

1 Included in A1

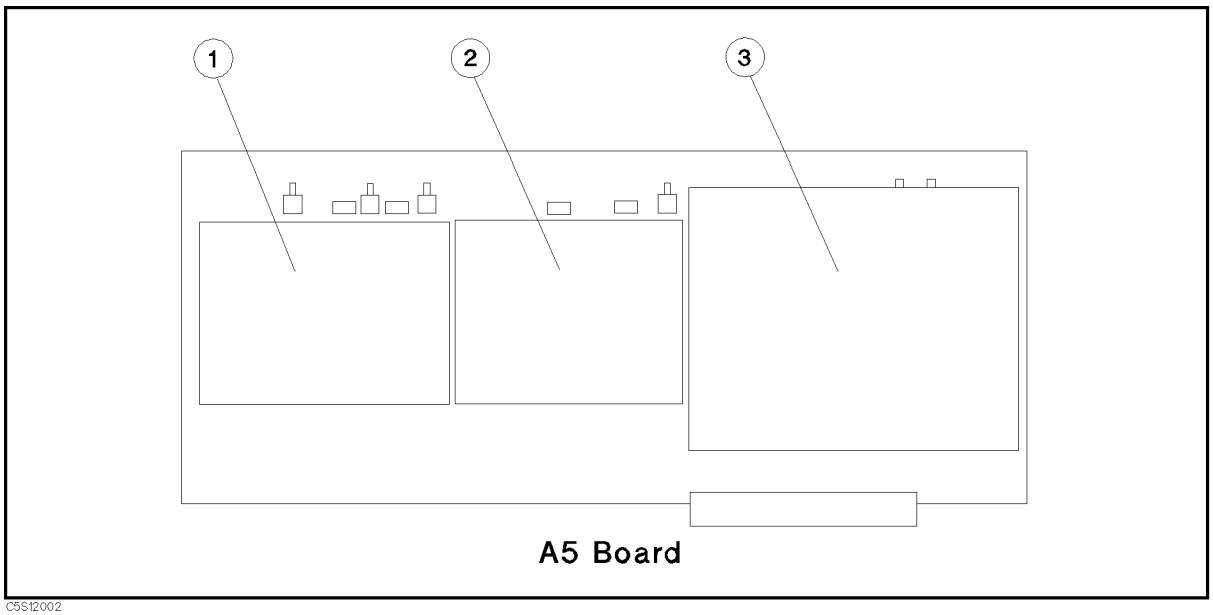


Figure 12-18. Miscellaneous Parts 4 (On A5)

Table 12-19. Miscellaneous Parts 4 (On A5)

Ref. Desig.	HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
1	04396-00651	8	1	Case Shield Component Side	28480	04396-00651
	04396-00652	9	1	Case Shield Component Side	28480	04396-00652
	0515-0914	8	4	Screw M3	28480	0515-0914
2	04396-00653	0	1	Case Shield Component Side	28480	04396-00653
	04396-00654	1	1	Case Shield Component Side	28480	04396-00654
	0515-0914	8	7	Screw M3	28480	0515-0914
3	04396-00655	2	1	Case Shield Component Side	28480	04396-00655
	04396-00656	3	1	Case Shield Component Side	28480	04396-00656
	0515-0914	8	4	Screw M3	28480	0515-0914

Parts listed in Table 12-19 are included in A5.

Table 12-20. Miscellaneous Parts 5 (Other Shields)

HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
04286-00601	5	1	Plate Shield Top	28480	04286-00601
8160-0694	6	4 cm	Gasket (for Plate Shield)	12085	UC300275
8160-0781	2	3 cm	Gasket (for Plate Shield)	12085	UC300227
0515-0913	7	3	Screw M4 (for Plate Shield)	28480	0515-0913
0515-0914	8	13	Screw M3 (for Plate Shield)	28480	0515-0914
04286-00606	0	1	CRT Plate Shield	28480	04286-00606
0515-1550		6	Screw M3 (for CRT Plate Shield)	28480	0515-1550
04396-00632	5	1	Case Shield (A3A1 Circuit Side)	28480	04396-00632
0515-1005	0	4	Screw M3 (for Case Shield)	28480	0515-1005
8160-0512	7	23cm	Gasket in A3A2 Case Shield	28480	8160-0512
0515-1550	0	4	Screw M3 (for A3A2)	28480	0515-1550
04291-00625	0	1	Case Shield (A6 Component Side)[1]	28480	04291-00625
04291-00626	1	1	Case Shield (A6 Circuit Side)[1]	28480	04291-00626
0515-0914	8	5	Screw M3 (for Case Shield)[1]	28480	0515-0914
0515-0914	8	5	Screw M3 (for Case Shield)[1]	28480	0515-0914
0515-1550	0	4	Screw M3	28480	0515-1550
08751-00643	7	1	Case Shield (A51 Component Side)[2]	28480	08751-00643
08751-00644	8	1	Case Shield (A51 Circuit Side)[2]	28480	08751-00644
0515-1550	0	4	Screw M3 (for Case Shield)[2]	28480	0515-1550

1 Included in A6

2 Included in A51

Table 12-21. Miscellaneous Parts 6 (Accessories)

HP Part Number	C D	Qty.	Description	Mfr Code	Mfr Part Number
See Figure B-2			Power Cable		
1250-1746	5	1	APC3.5(m)-APC7 Adapter	05879	131-91045-1001
1250-1249	3	1	APC3.5(m)-APC3.5(f) Right Angle Adapter[1]	16179	2088-0000-00
04286-60141	4	1	Test fixture Stand[2]	28480	04286-60141
46021-60401	9	1	HP-HIL Keyboard[3]	28480	46021-60401
46020-60001	3	1	Cable for Keyboard[3]	28480	46020-60001
08751-87111	6	1	Template for Keyboard[3]	28480	08751-87111
			Calibration Kit[4]		
04191-85302	7	1	0 S Termination	28480	04191-85302
04191-85300	5	1	0 Ω Termination	28480	04191-85302
16195-65006[5]	2	1	50 Ω Termination	28480	16195-65006
04291-60042	1	1	Low-loss Capacitor	28480	04291-60042
16195-60001	0	1	Carrying Case	28480	16195-60001
			Working Standard Set[6]		
16191-29005	4	1	Short Bar 1.0 × 0.5 mm	28480	16191-29005
16191-29006	5	1	Short Bar 1.6 × 0.8 mm	28480	16191-29006
16191-29007	6	1	Short Bar 2.0 × 1.25 mm	28480	16191-29007
16191-29008	7	1	Short Bar 3.2 × 1.6 mm	28480	16191-29008
5182-0433	4	5	51 Ω Resistor 1.0 × 0.5 mm	28480	5182-0433
5182-0434	5	5	51 Ω Resistor 1.6 × 0.8 mm	28480	5182-0434
5182-0435	6	5	51 Ω Resistor 2.0 × 1.25mm	28480	5182-0435
5182-0436	7	5	51 Ω Resistor 3.2 × 1.6 mm	28480	5182-0436
1540-0692	3	5	Case	28480	1540-0692
			Service Software		
04286-65002	6		Adjustment Program[7]	28480	04286-65002
			Documentation		
04286-90000	7		Operating Manual Set	28480	04286-90000
04286-90007	4		Programing Manual Set	28480	04286-90007
E2083-90000	5		HP IBASIC Handbook[3]	28480	E2083-90000
04286-90005	9		HP IBASIC Handbook Supplement[3]	28480	04286-90005
04286-90101	9		Service Manual[8]	28480	04286-90101

1 Option 021/022 only

2 Not furnished with option 002

3 Option 1C2 only

4 Not furnished with option 001

5 *Calibration Kit Contents List* must be filled out in the 50 Ω replacement.

6 Option 004 only

7 Not furnished

8 Option 0BW only

13

Replacement Procedures

INTRODUCTION

This chapter describes how to replace the analyzer's major assemblies. The cover and panel removal procedures that are required for some assembly replacements are described first. Then the replacement procedures for each major assembly is described.

TOP COVER REMOVAL

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #2 (medium)

Procedure

1. Disconnect the power cable from the HP 4286A.
2. Remove the two rear feet behind the top cover.
3. Loosen the top cover rear screw.
4. Slide the top cover toward the rear and lift it off.

BOTTOM COVER REMOVAL

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #2 (medium)

Procedure

1. Disconnect the power cable from the HP 4286A.
2. Place the HP 4286A upside down.
3. Remove the two rear feet behind the bottom cover.
4. Loosen the bottom cover rear screw.
5. Slide the bottom cover toward the rear and lift it off.

SIDE COVER REMOVAL

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #2 (medium)

Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the bottom cover as described in the "BOTTOM COVER REMOVAL" procedure.
3. Remove the two screws at the side strap handle caps to remove the strap.
4. Slide off the side cover toward the rear.
5. For the other side cover, repeat steps 3 and 4.

FRONT PANEL REMOVAL

Tools Required

- Pozidriv screwdriver, pt size #2 (medium)
- Flat blade screwdriver.

Procedure

1. Place the HP 4286A upside down.
2. Remove the two front feet.
3. Remove the four screws designated ① in Figure 13-1 from the bottom of the front frame.

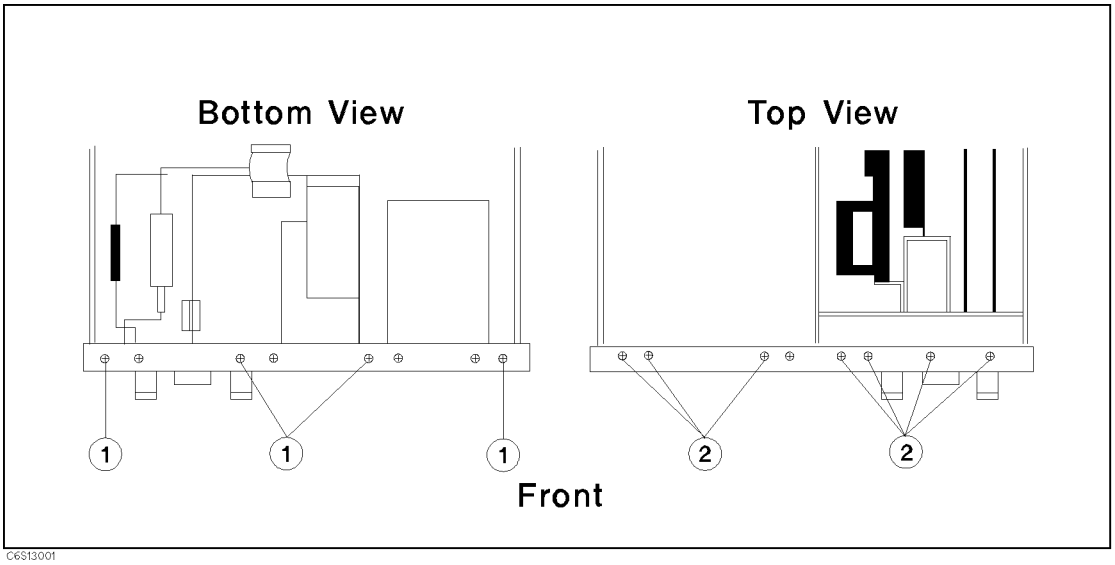


Figure 13-1. Front Panel Screws

4. Turn the HP 4286A over into the correct position.
5. Remove the top trim strip from the front frame by prying the trim strip up with a flat screwdriver.
6. Remove the seven screws designated ② in Figure 13-1 from the top of the front frame.
7. Gently pull the front panel knob to remove the front panel assembly from the front frame.

REAR PANEL REMOVAL

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdrivers, pt size #1 (small), size #2 (medium)

Procedure

1. Remove the top, bottom, and side covers as described in the "SIDE COVER REMOVAL" procedure.
2. Place the HP 4286A upside down.
3. Remove the three screws designated ① in Figure 13-2.

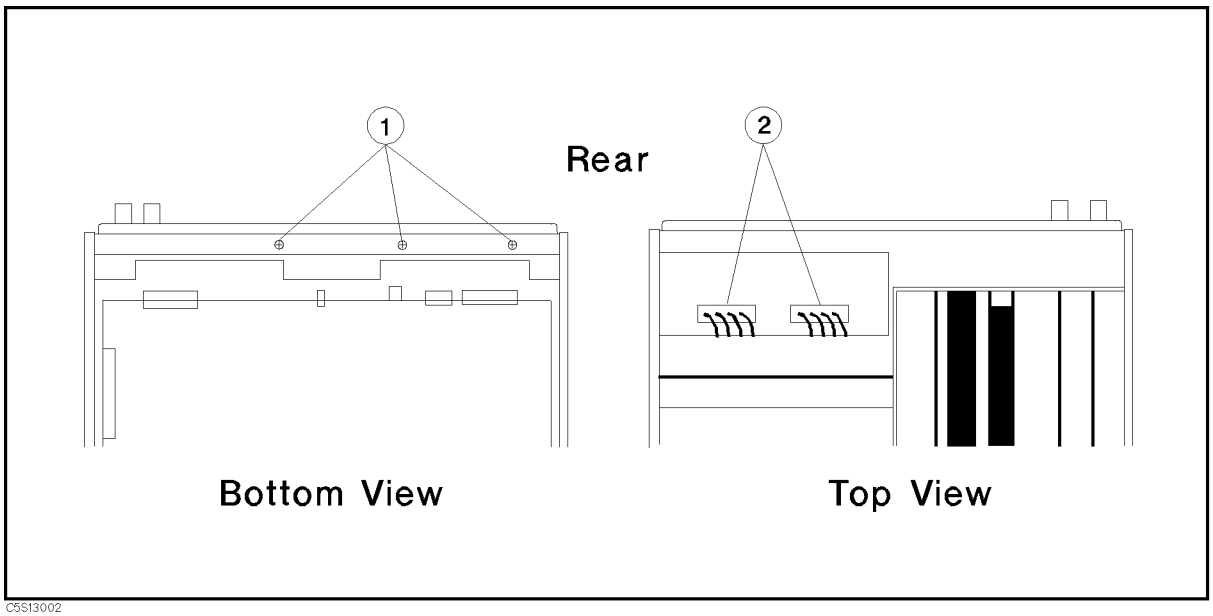


Figure 13-2. Rear Panel Assembly Removal

4. Turn the HP 4286A over into the correct position.
5. Remove the top shield plate.
6. Disconnect the two cables designated ② in Figure 13-2.
7. Remove the RF flexible cables "I" and "O" from A5 Synthesizer.
8. Remove the RF cable "V" from A60 Frequency Reference (Option 1D5.)
9. Gradually push the A40 preregulator toward the rear to pull the rear panel assembly out from the rear frame, and remove the all cables connected to the rear panel.

A1 CPU REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)
- IC Extractor

Removal Procedure

1. Remove the bottom cover as described in the "BOTTOM COVER REMOVAL" procedure.
2. Disconnect all cables and wires from A1.
3. Remove the EEPROM from A1. Mount the EEPROM on the replacement A1.

Note When using a re-built A1, return the defective A1 with the EEPROM originally mounted on the re-built A1.

4. Remove all screws (13 ea.) from A1 to remove A1 from the chassis.

Replacement Procedure

1. Place the replacement A1 on the HP 4286A.
2. Attach A1 with the screws removed in the "Removal Procedure" procedure.
3. Connect all cables disconnected in the "Removal Procedure" to A1.
4. Replace the bottom cover.

A2 POST REGULATOR REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small)

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Disconnect the wire "2" (A2 - A40).
4. Remove the three screws on the A2 heat sink.
5. Lift the extractors at the top of A2, and lift A2 out.
6. Disconnect the wire "3" (A2 - A51/A52).

Replacement Procedure

Reverse the "Removal Procedure" to replace A2.

A3A1 Source Vernier, A3A2 SECOND LO, AND A3A3 SOURCE REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)
- Open-end wrench, 1/4 inch and 5/16 inch

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Remove the semi rigid cables "C" and "I" completely from the HP 4286A.
4. Remove the semi rigid cable "D" from A3A3, and clamp the cable with the cable clamp on the chassis. (The cable needs to be clamped so that the cable is not caught by A3 when A3 is lifted out.)
5. Disconnect the flexible cable "J" from A3A1.
6. Remove the two screws at the top corners of A3A2.
7. Lift the extractors at the top of A3A1, and lift A3 out.
8. *—A3A1 Removal—*
   a. Remove all cables and wires from A3A1.
   b. Place A3 facing A3A1 upward as shown in Figure 13-3.

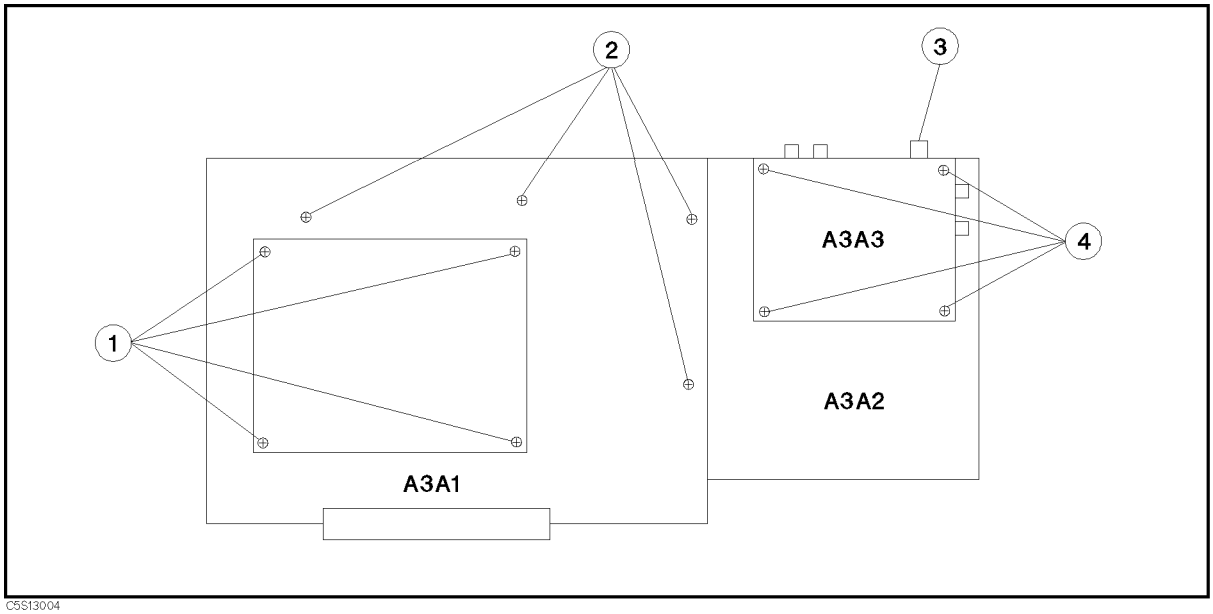


Figure 13-3. A3A1, A3A2, and A3A3 Replacement

c. Remove the four screws designated ① in Figure 13-3 to remove the shield case on A3A1.

d. Remove the four screws designated ② in Figure 13-3 to remove A3A1 from A3A2.

Note When using a re-built A3A1, return the defective A3A1 without the shield case.

9. *—A3A2 Removal—*

a. Remove all cables from A3A2.

b. Remove A3A1 as described in *A3A1 Removal.*

c. Remove A3A3 as described in *A3A3 Removal.*

d. Pull the gasket out from A3A2 shield, and install the gasket in the replacement A3A2.

Note When using a re-built A3A2, return the defective A3A2 without the gasket.

10. *—A3A3 Removal—*

a. Place A3 facing A3A2 upward as shown in Figure 13-3.

b. Remove all cables and wires from A3A3.

c. Remove the connector cover designated ③ in Figure 13-3.

d. Remove the four screws designated ④ in Figure 13-3 to remove A3A3 from A3A2.

Replacement Procedure

Reverse the “Removal Procedure” to replace A3A1, A3A2, and A3A3.

A4 FIRST LO/RECEIVER RF REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)
- Open-end wrench, 1/4 inch and 5/16 inch

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Remove the semi rigid cables "C", "F" and "I" completely from the HP 4286A.
4. Disconnect the flexible cables "H_1", "H_2", "L", and "M" from A4.
5. Remove the two screws at the top corners of A4, and lift A4 out.

Note A4A1 First LO and A4A2 Receiver RF must not be separated.

Replacement Procedure

Reverse the "Removal Procedure" to replace A4.

A5 SYNTHESIZER REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small)
- Open-end wrench, 1/4 inch

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Disconnect all cables from A5.
4. Lift the extractors at the top of A5, and lift A5 out.

Replacement Procedure

Reverse the "Removal Procedure" to replace A5.

A6 RECEIVER IF REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small)

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Disconnect the flexible cable "M" from A6.
4. Lift the extractors at the top of A6 to disconnect the flexible cable "F" from A6.
5. Lift A6 out.

Replacement Procedure

Reverse the "Removal Procedure" to replace A6.

A7 OUTPUT ATT AND A8 3 dB ATT REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)
- Open-end wrench, 5/16 inch

Removal Procedure

1. Remove the bottom cover as described in the "BOTTOM COVER REMOVAL" procedure.
2. Remove the flexible cable "F" from A8.
3. Remove A8 from A7.
4. Unsolder the wire "9" (A7 - A20) from the A7.
5. Remove the semi rigid cable "D" from A7.
6. Remove the two screws to remove the A7 holder from the chassis.
7. Remove the two screws to remove A7 from the holder.

Replacement Procedure

Reverse the "Removal Procedure" to replace A7 or A8. In connecting the cables.

A30 KEYBOARD REPLACEMENT

Tools Required

- Pozidriv screwdrivers, pt size #1 (small) and #2 (medium)
- Flat blade screwdriver

Removal Procedure

1. Remove the front panel as described in the "FRONT PANEL REMOVAL" procedure.
2. Disconnect the flat cable assembly from A30.
3. Remove the eight screws on A30 to remove A30 from the front panel.

Replacement Procedure

Reverse the "Removal Procedure" to replace A30.

A33 HANDLER INTERFACE/BACKUP SRAM REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #2 (medium)

Removal Procedure

1. Disconnect the flexible cable "H" from A4 and A5.
2. Disconnect the flexible cable "E" and "N" from A33.
3. Remove two screws at the top corners of A33.
4. Lift A33 out.

Replacement Procedure

Reverse the "Removal Procedure" to replace A33.

A40 PREREGULATOR REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #2 (medium)

Removal Procedure

1. Remove the rear panel as described in the "REAR PANEL REMOVAL" procedure.
2. Place the rear panel assembly facing the panel to you.
3. Remove the four screws that fix A40 while holding A40.
4. Remove A40 from the rear panel.

Replacement Procedure

Reverse the "Removal Procedure" to replace A40.

A43 HEAD CONTROL REPLACEMENT

Tools Required

- Pozidriv screwdriver, pt size #1 (small)

Removal Procedure

1. Remove the eight screws which hold two N(m)-SMA(f) adapters.
2. Remove the test head top cover.
3. Disconnect the flexible cables from A43J1, J6 and J7.
4. Disconnect the wires from A43J3 and J5.
5. Remove the screws on A43, and remove A43 from the test head bottom cover.

Replacement Procedure

Reverse the "Removal Procedure" to replace A43.

1m/3m CABLE ASSEMBLY REPLACEMENT

Tools Required

- Pozidriv screwdriver, pt size #1 (small)

Removal Procedure

1. Remove the eight screws which hold two N(m)-SMA(f) adapters.
2. Remove the test head top cover.
3. Disconnect the flexible cables from A43J6 and J7.
4. Disconnect the wire from A43J5.
5. Remove the cable clamp and cable tie, and remove the 1m/3m cable assembly from A43.

Replacement Procedure

Reverse the "Removal Procedure" to replace the cable assembly.

Note

When replacing the test head assembly (or when replacing the assembly that contains the serial number label) the serial number is required to identify the test head and guarantee the HP 4286A system specifications. The serial number label is either on the test head bottom cover or the side panel of the 1m/3m cable assembly. Because the new assembly does not have a serial part number, you must remove the old part that contains the serial number (either the bottom cover or the side panel) and install it on the new assembly before replacing the test head assembly.

A51 GSP REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Remove all cables from the top of A51.
4. Lift the extractors at the top of A51, and lift A51 out.

Replacement Procedure

Reverse the "Removal Procedure" to replace A51.

A52 DC-DC CONVERTER REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small) and #2 (medium)

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the top shield plate.
3. Remove all cables from the top of A52.
4. Lift the extractors at the top of A52, and lift A52 out.

Replacement Procedure

Reverse the "Removal Procedure" to replace A52.

CRT REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdrivers, pt size #1 (small) and #2 (medium)

Removal Procedure

1. Remove the top cover as described in the "TOP COVER REMOVAL" procedure.
2. Remove the front panel as described in the "FRONT PANEL REMOVAL" procedure.
3. Remove the top shield plate.
4. Remove the top shield over the CRT.
5. Disconnect the flat cable from A52 converter.
6. Remove the four screws which hold the CRT.
7. Pull the CRT out toward the front.

Replacement Procedure

Reverse the "Removal Procedure" to replace the CRT.

FLEXIBLE DISK DRIVE REPLACEMENT

Tools Required

- Torx screwdriver, T15
- Pozidriv screwdriver, pt size #1 (small)
- Hex socket, 7/32 inch (5.5 mm)

Removal Procedure

1. Remove the bottom cover as described in the "BOTTOM COVER REMOVAL" procedure.
2. Remove the flat cable from the cable clamp on the FDD holder.
3. Disconnect the FDD's flat cable from the A1 CPU.
4. Remove the four nuts from the FDD holder.
5. Remove the FDD with the holder from the chassis.
6. Remove the four screws from the holder to remove it from the FDD.
7. Disconnect the flat cable and wire from the FDD.

Replacement Procedure

Reverse the "Removal Procedure" to replace A53.

14

Post Repair Procedures

INTRODUCTION

This chapter lists the procedures required to verify the HP 4286A operation after an assembly is replaced with a new one.

POST REPAIR PROCEDURES

Table 14-1 *Post Repair Procedures* lists the required procedures that must be performed after the replacement of an assembly or the EEPROM. These are the recommended minimum procedures to ensure that the replacement is successfully completed.

When you replace an assembly or the EEPROM on the A1 CPU, perform the adjustments and updating correction constants (CC), then verify the HP 4286A performance according to Table 14-1.

For the detailed procedure of the adjustments and updating correction constants, see Chapter 3. For the detailed verification procedures, see this manual's chapter specified in Table 14-1.

Table 14-1. Post Repair Procedures

Replaced Assembly or Part	Adjustments Correction Constants (CC)	Verification
A1 CPU	Firmware Installation.[1]	*INSPECT THE POWER ON SEQUENCE* [2] Internal Test 2: A1 VOLATILE MEMORY[3]
A1 EEPROM	OSC Level CC	*INSPECT THE POWER ON SEQUENCE*[2] *OSC Level Accuracy Test*[4]
A2 Post-Regulator		*INSPECT THE POWER ON SEQUENCE*[2] Frequency Accuracy Test[4]
A3A1 Source Vernier	Source VCXO Adjustment OSC Level CC	*INSPECT THE POWER ON SEQUENCE* [2] *OSC Level Accuracy Test* [4] External Test 23: FRONT ISOL'N[3]
A3A2 2nd LO	Second LO PLL Lock Adjustment Source Mixer Local Leakage Adjustment OSC Level CC	*INSPECT THE POWER ON SEQUENCE* [2] *OSC Level Accuracy Test* [4] External Test 23: FRONT ISOL'N[3]

1 See the *Firmware Installation* procedure in this chapter.

2 See Chapter 4.

3 See Chapter 10.

4 See Chapter 2.

Table 14-1. Post Repair Procedures (continued)

Replaced Assembly or Part	Adjustments Correction Constants (CC)	Verification
A3A3 Source	OSC Level CC	*INSPECT THE POWER ON SEQUENCE* [1] *OSC Level Accuracy Test* [2] External Test 23: FRONT ISOL'N [3]
A4 1st LO/Receiver RF	None	*INSPECT THE POWER ON SEQUENCE* [1] External Test 23: FRONT ISOL'N [3]
A5 Synthesizer	40 MHz Reference Oscillator Adjustment 520 MHz Level Adjustment Comb Generator Adjustment	*INSPECT THE POWER ON SEQUENCE* [1] *Frequency Accuracy Test* [2]
A6 Receiver IF	Source VCXO Adjustment Hold Step Adjustment Band Pass Filter Adjustment	*INSPECT THE POWER ON SEQUENCE* [1]
A7 Output ATT	OSC Level CC	*INSPECT THE POWER ON SEQUENCE* [1] External Test 19: OUTPUT ATTENUATOR [3] *OSC Level Accuracy Test* [2]
A8 Output 3 dB ATT	OSC Level CC	*OSC Level Accuracy Test* [2]
A9 Input 3 dB ATT	None	External Test 20: RECEIVER GAIN [3]
A20 Motherboard	None	*INSPECT THE POWER ON SEQUENCE* [1]
A30 Keyboard	None	*INSPECT THE POWER ON SEQUENCE* [1] External Test 16: FRONT PANEL DIAG. [3]
A31 I/F Connector	None	*TROUBLESHOOT HP-IB SYSTEM* [1] External Test 25:A33 HANDLER IF
A32 I-BASIC Interface	None None	*INSPECT THE POWER ON SEQUENCE* [1] *Check the A32 I-BASIC Interface and HP-HIL Key board* [4]
A33 Handler I/F with Backup SRAM	None	External Test 25: A33 HANDLER IF Internal Test 15: A33 Memory Disk
A40 Pre-Regulator	None	Internal Test 4: A2 POST REGULATOR [3]
Test Head	None	*INSPECT THE POWER ON SEQUENCE* [1] External Test 24: TEST HEAD
A51 GSP	None	*INSPECT THE POWER ON SEQUENCE* [1]
CRT	None	*INSPECT THE POWER ON SEQUENCE* [1]
FDD	None	*INSPECT THE POWER ON SEQUENCE* [1] External Test 17: DSK DR FAULTY ISOLN [3]

1 See Chapter 4.

2 See Chapter 2.

3 See Chapter 10.

4 See Chapter 6.

FIRMWARE INSTALLATION

No firmware is installed in new A1 CPU assembly (PN 04396-66501 or PN 04396-69501 for a rebuilt exchange). When you replace a faulty A1 CPU with a new one, perform the following steps to install the firmware into the A1 CPU.

Ordering the Firmware Diskette

A firmware diskette (3.5 inch) that contains the HP 4286A's firmware is required for the firmware installation. If you do not have a firmware diskette, you must order one. For ordering information, contact your nearest Hewllet-Packard service center and provide the revision of the HP 4286A's firmware. The part number of the firmware diskette depends on the firmware revision. The firmware revision of the HP 4286A is indicated on the revision label attached on the rear panel as shown in Figure 14-1.

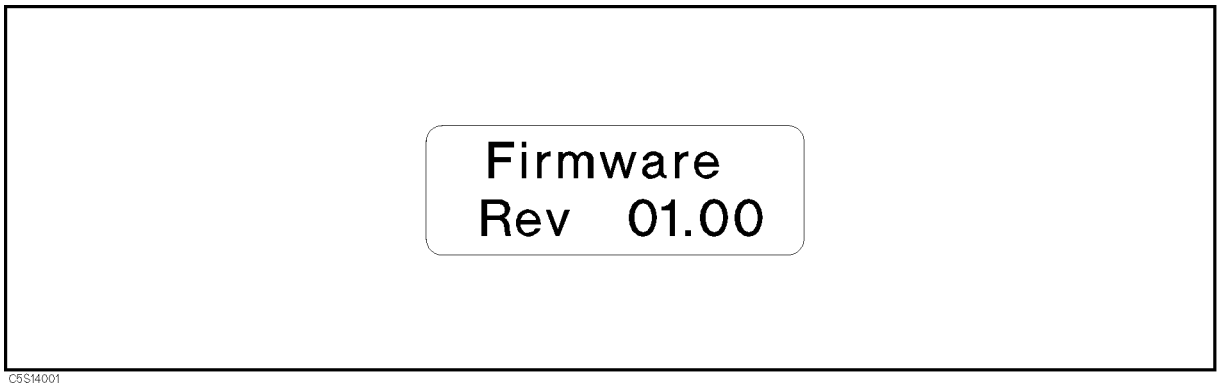


Figure 14-1. Firmware Revision Label

Installing the Firmware

Perform the following procedure to install the firmware into the HP 4286A.

1. Turn the HP 4286A power off.
2. Press both the [Trigger] and [Preset] keys. While pressing both keys, turn the HP 4286A power on.
3. Wait until the bootloader menu appears on the CRT as shown in Figure 14-2.

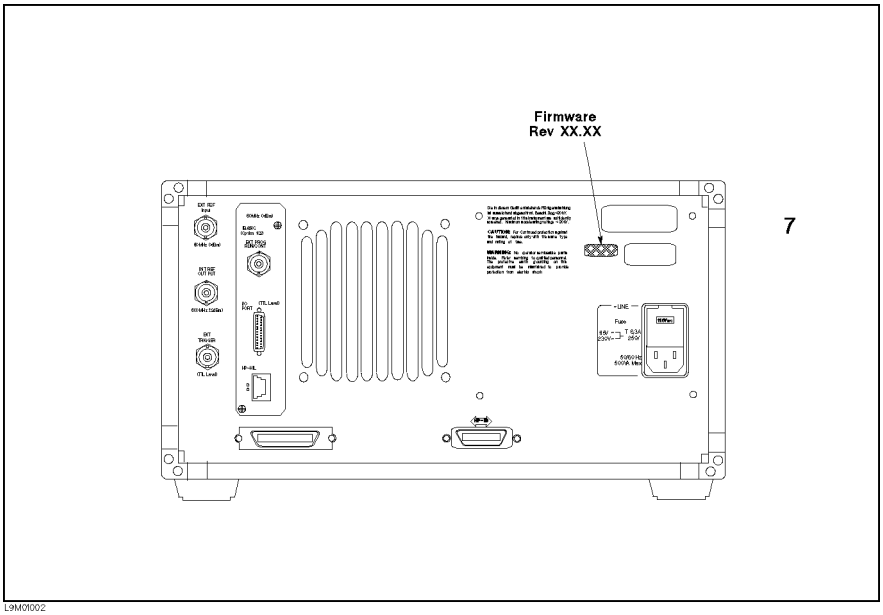


Figure 14-2. Bootloader Menu Display

4. Insert the firmware diskette into the floppy disk drive on the front panel.
5. Press `SYSTEM UPDATE` and `CONTINUE`. The HP 4286A displays "Loading From Disk" and starts the firmware installation.
6. Wait until the HP 4286A displays "Update Complete."
7. Press `REBOOT` or turn the HP 4286A power off and on. The HP 4286A starts the operation using the installed firmware.
8. Verify that no error message is displayed and that the revision displayed is that of the revision label.
   - In case of unexpected results, inspect the firmware diskette for any damage. Clean the built-in FDD and retry the procedure.

A

Manual Changes

Introduction

This appendix contains the information required to adapt this manual to earlier versions or configurations of the HP 4286A than the current printing date of this manual. The information in this manual applies directly to the HP 4286A RF LCR Meter serial number prefix listed on the title page of this manual.

Manual Changes

To adapt this manual to your HP 4286A, refer to Table A-1 and Table A-2, and make all of the manual changes listed opposite your instrument's serial number and firmware version.

Instruments manufactured after the printing of this manual may be different than those documented in this manual. Later instrument versions will be documented in a manual changes supplement that will accompany the manual shipped with that instrument. If your instrument's serial number is not listed on the title page of this manual or in Table A-1, it may be documented in a *yellow MANUAL CHANGES* supplement.

Turn on the line switch or execute the "`*IDN?`" command by HP-IB to confirm the firmware version. See *HP-IB Command Reference* for information on the "`*IDN?`" command. For additional information on serial number coverage, see chapter 1 of the *Function Reference*.

Table A-1. Manual Changes by Serial Number

Serial Prefix or Number	Make Manual Changes

Table A-2. Manual Changes by Firmware Version

Version	Make Manual Changes

Serial Number

Hewlett-Packard uses a two-part, ten-character serial number that is stamped on the serial number plate (see Figure A-1) attached to the rear panel. The first ive digits are the serial prefix and the last five digits are the suffix.

Figure A-1. Serial Number Plate

B

Power Requirement

Power Requirements

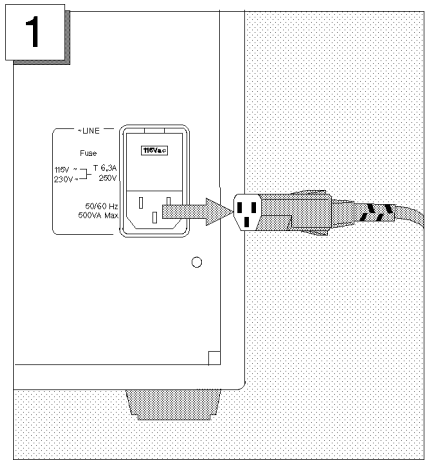
The HP 4286A can operate from any single phase ac power source supplying 90 V to 132 V, or 198 V to 264 V in the frequency range from 47 to 66 Hz (see Table B-1). With all options installed, the power consumption is less than 500 VA.

Table B-1. Line Voltage Ranges

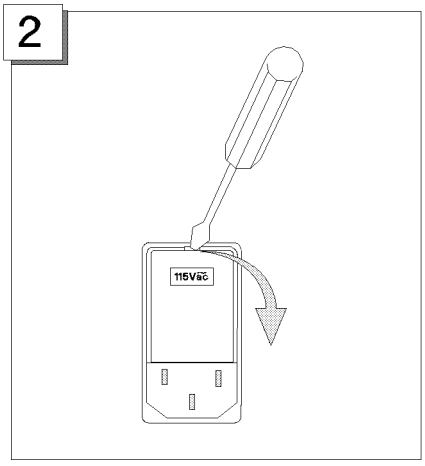
AC Voltage Range	Selector Voltage
90 V to 132 V	115 V
198 V to 264 V	230 V

Changing the Line Voltage Setting

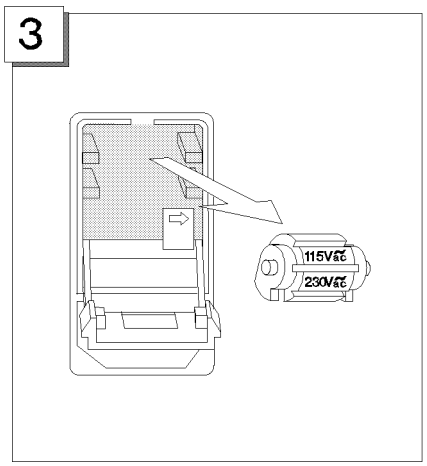
The line voltage selector is set at the factory to correspond to the most commonly used line voltage of the country of destination. The line voltage selected for the HP 4286A is indicated on the line voltage selector. Refer to table Table B-1 for the line voltage ranges. Perform the following steps to change the line voltage:



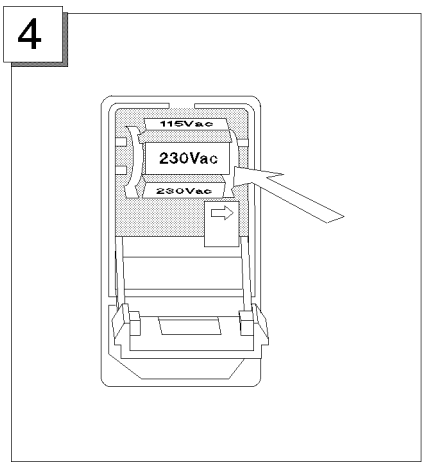
Remove the power cord if it is connected.



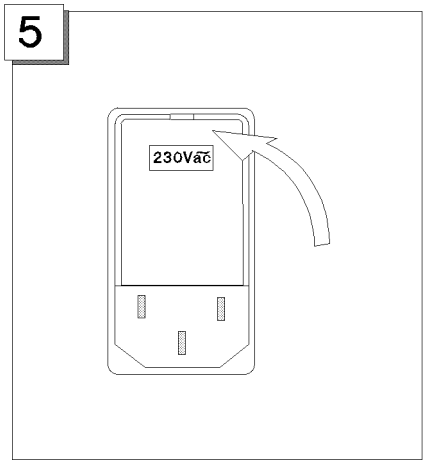
Open the cover of AC line receptacle on the rear panel using a small, flat-blade screwdriver.



Pull out the Line-Voltage Drum.



Insert the Line-Voltage Drum so that the required voltage is displayed at the front.



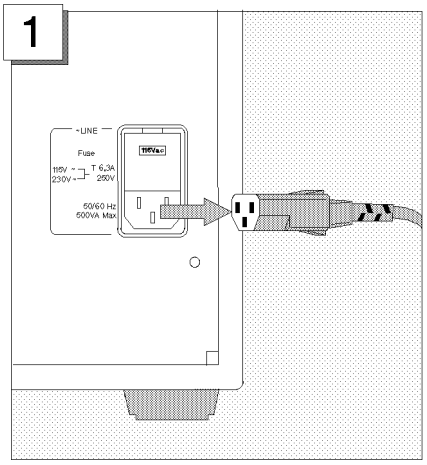
Close the cover by pushing it until it clicks. Verify that the correct line voltage appears in the window of the power selector cover.

Replacing the Fuse

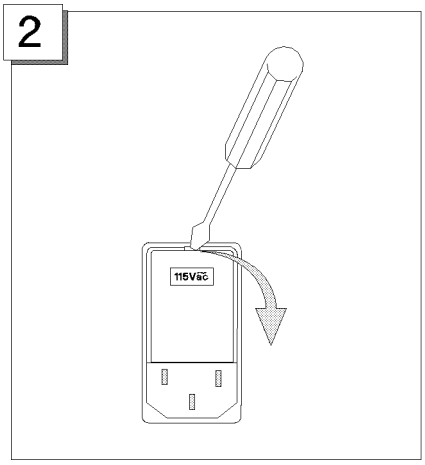
The HP part number of the fuse is 2110-0917.

Note The same fuse can be used for both line voltage settings. You do not have to change the fuse when changing the line voltage.

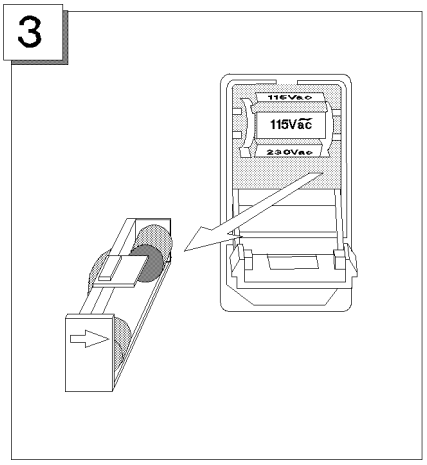
Perform the following steps to exchange the fuse.



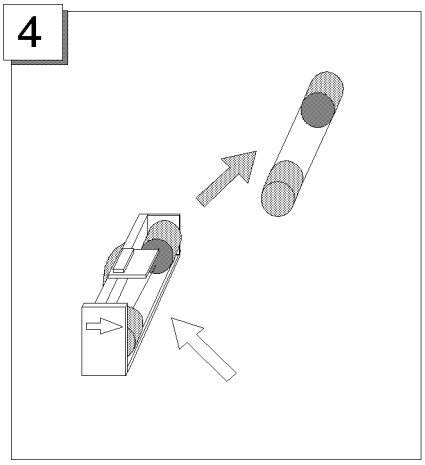
Remove the power cord if it is connected.



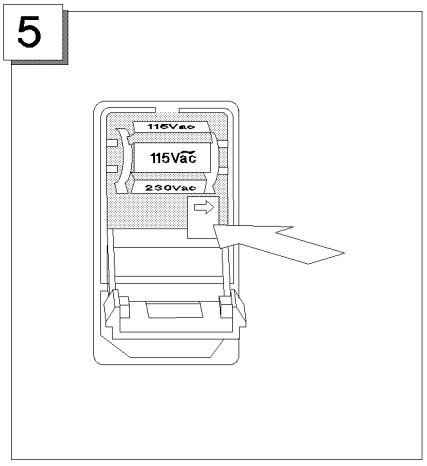
Open the cover of AC line receptacle on the rear panel using a small, flat-blade screwdriver.



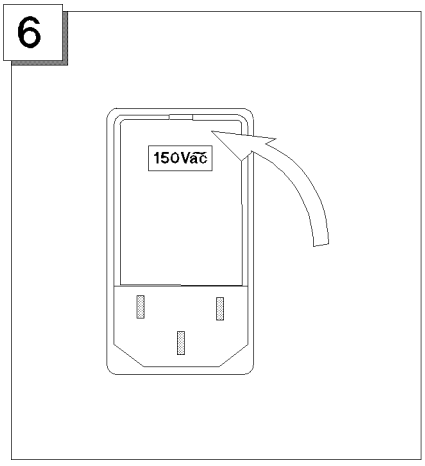
To check or replace the fuse, pull the fuse holder out of the power selector and remove the fuse from the fuse holder.



To reinstall the fuse, insert a fuse into the fuse holder.



Push the fuse holder into the power selector.



Close the cover by pushing it until it clicks.

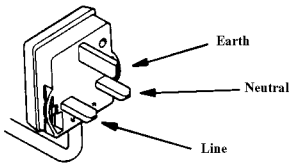
Power Cable Requirement

The HP 4286A is equipped with a three-conductor power cord that, when plugged into an appropriate receptacle, grounds the HP 4286A cabinet. To protect operating personnel, the offset pin on the power cord must be grounded so that the instrument panel and cabinet are grounded.

To preserve this protection feature when operating the instrument from a two-prong outlet, use a three-prong to two-prong adapter (HP Part Number 1251-8196) and connect the green pigtail on the adapter to the power-line ground.

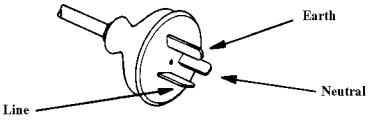
Figure B-1 shows the available power cords used in various countries. Also shown is the standard power cord furnished with the instrument. HP part numbers, applicable standards for power plugs, electrical characteristics, and the countries using each type of power cord are also listed in Figure B-1. For assistance in selecting the correct power cord, contact the nearest Hewlett-Packard sales office.

OPTION 900 United Kingdom



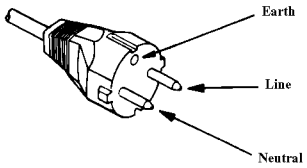
Plug : BS 1363A, 250V
Cable : HP 8120-1351

OPTION 901 Australia / New Zealand



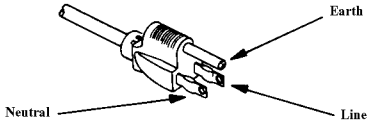
Plug : NZSS 198/AS C112, 250V
Cable : HP 8120-1369

OPTION 902 European Continent



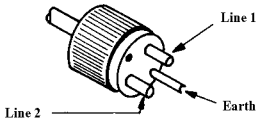
Plug : CEE-VII, 250V
Cable : HP 8120-1689

OPTION 903 U.S. / Canada



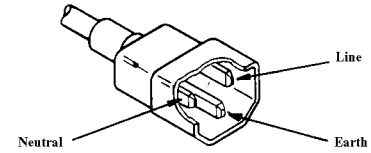
Plug : NEMA 5-15P, 125V, 15A
Cable : HP 8120-1378

OPTION 904 U.S. / Canada



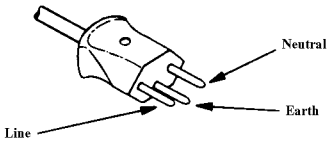
Plug : NEMA 6-15P, 250V, 15A
Cable : HP 8120-0698

OPTION 905* Any country



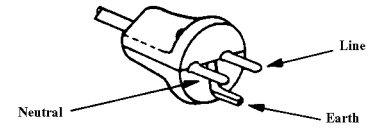
Plug : CEE 22-VI, 250V
Cable : HP 8123-1396

OPTION 906 Switzerland



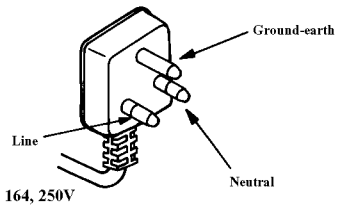
Plug : SEV 1011.1959-24507 Type 12, 250V
Cable : HP 8120-2104

OPTION 912 Denmark



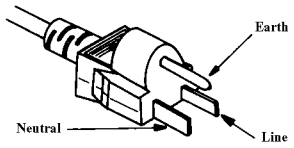
Plug : DHCR 107, 220V
Cable : HP 8120-2956

OPTION 917 India / Republic of S.Africa



Plug : SABS 164, 250V
Cable : HP 8120-4211

OPTION 918 Japan



Plug : JIS C 8303, 125V, 15A
Cable : HP 8120-4753

NOTE: Each option number includes a 'family' of cords and connectors of varoius materials and plug body configurations (straight, 90° etc.).

* Plug option 905 is frequently used for interconnecting system components and peripherals.

Figure B-1. Power Code Supplied

Error Messages

This section lists the service related error messages that may be displayed on the HP 4286A display or transmitted by the instrument over HP-IB. Each error message is accompanied by an explanation, and suggestions are provided to help in solving the problem.

When displayed, error messages are usually preceded with the word CAUTION:. That part of the error message has been omitted here for the sake or brevity. Some messages are for information only, and do not indicate an error condition. Two listings are provided: the first is in alphabetical order, and the second in numerical order.

Error Messages in Alphabetical Order

222 **1st LO OSC TEST FAILED**

The 1st LO OSC (first local oscillator) on the A4A1 1st LO does not work properly. This message is displayed when an internal test 8: A4A1 1ST LO OSC fails. Troubleshoot the source group in accordance with Chapter 7.

223 **2nd LO OSC TEST FAILED**

The 2nd LO OSC (second local oscillator) on the A3A2 2nd LO does not work properly. This message is displayed when an internal test 9: A3A2 2ND LO fails. Troubleshoot the source group in accordance with Chapter 7.

225 **3rd LO OSC TEST FAILED**

The 3rd LO OSC (third local oscillator) on the A6 receiver IF does not work properly. This message is displayed when an internal test 11: A6 3RD LO OSC fails. Troubleshoot the receiver group in accordance with Chapter 8.

224 **A3 DIVIDER OUTPUT FREQUENCY OUT OF SPEC**

The output frequency of the divider circuit on the A3A1 ALC is out of its limits. This message is displayed when an internal test 10: A3A1 DIVIDER fails. Troubleshoot the source group in accordance with Chapter 7.

243 **A6 GAIN TEST FAILED**

An “external test 21: A6 GAIN” fails. Replace the A6 receiver IF. See Chapter 8.

244 **A6 VI NORMALIZER TEST FAILED**

An “external test 22: A6 VI NORMALIZER” fails. Replace the A6 receiver IF. See Chapter 8.

200 **ALL INT TEST FAILED**

This message is displayed when an internal test 0: ALL INT fails. Troubleshoot the HP 4286A in accordance with Chapter 4.

202 **BACKUP SRAM CHECK SUM ERROR**

The data (HP-IB Address and so on) stored in the A1 CPU's BACKUP SRAM are invalid. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

190 **CORR. CONST. DATA LOST; DEFAULT DATA IS USED**

This message is displayed when the correction constants EEPROM data is lost and turned on in the service mode. Troubleshoot the HP 4286A in accordance with Chapter 6 .

212 **CPU BACKUP SRAM R/W ERROR**

The A1 CPU's BACKUP SRAM does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See Chapter 6 .

211 **CPU INTERNAL SRAM R/W ERROR**

The A1 CPU's internal SRAM does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See Chapter 6 .

204 **DSP CHIP TEST FAILED**

The A1 CPU's DSP (Digital Signal Processor) does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

213 **DSP SRAM R/W ERROR**

The DSP's SRAM on the A1 CPU does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 COU with a new one. See Chapter 6 .

214 **DUAL PORT SRAM R/W ERROR**

The DSP's dual port SRAM on the A1 CPU does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See Chapter 6 .

203 **EEPROM CHECK SUM ERROR**

The data (Correction Constants and so on) stored in the A1 CPU's EEPROM are invalid. This message is displayed when an internal test 1: A1 CPU fails. Troubleshoot the A1 CPU in accordance with Chapter 6 .

199 **EEPROM WRITE ERROR**

Data cannot be stored properly into the EEPROM on the A1 CPU. This message is displayed when performing the display background adjustment or updating correction constants in the EEPROM using the adjustment program. Troubleshoot the A1 CPU in accordance with Chapter 6 .

205 **F-BUS TIMER CHIP TEST FAILED**

The A1 CPU's F-BUS (Frequency Bus) timer does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

218 **FAILURE FOUND FROM A/D MUX TO A/D CONVERTER**

A trouble is found on the signal path from the A/D multiplexer to A/D converter on the A6 receiver IF. This message is displayed when an internal test 5: A6 A/D CONVERTER fails. Troubleshoot the A6 receiver IF in accordance with Chapter 8.

217 **FAN POWER OUT OF SPEC**

The voltage of the fan power supply at the DC bus node 11 is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with Chapter 5.

208 **FDC CHIP TEST FAILED**

The A1 CPU's FDC (Flexible Disk drive control) ship does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

201 **FLASH MEMORY CHECK SUM ERROR**

The data (Firmware) stored in the A1 flash memory are invalid. This message is displayed in the bootloader menu. Troubleshoot the A1 CPU in accordance with Chapter 6 .

230 **FLOPPY DISK DRIVE FAILURE FOUND**

The built-in FDD (Floppy Disk Drive) does not work properly. This message is displayed when an external test 17: DSK DR FAULT ISOL'N fails. Replace the FDD with a new one. See Chapter 6 .

220 **FRACTIONAL N OSC TEST FAILED**

The fractional N oscillator on the A5 synthesizer does not work properly. This message is displayed when an internal test 7: A5 FRACTIONAL N OSC fails. Troubleshoot the source group in accordance with Chapter 7.

239 **FRONT ISOL'N TEST FAILED**

An "external test 23: FRONT ISOL'N" fails. Troubleshoot the receiver group in accordance with Chapter 8.

216 **GND LEVEL OUT OF SPEC**

The voltage of the GND (Ground) at the DC bus node 26 is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with Chapter 5.

210 **HP-HIL CHIP TEST FAILED**

The A1 CPU's HP-HIL control chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

209 **HP-IB CHIP TEST FAILED**

The A1 CPU's HP-IB chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

207 **KEY CHIP TEST FAILED**

The A1 CPU's front keyboard control chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

245 **MAX VCXO LEVEL OUT OF SPEC**

Maximum VCXO level is incorrect, in performing an "adjustment test 28: 3RD VCXO LEVEL ADJ" or an "adjustment test 31: SOURCE VCXO LEVEL ADJ". In the 3RD VCXO LEVEL ADJ, replace the A6 receiver IF. In the SOURCE VCXO LEVEL ADJ, replace the A3A1 source vernier.

233 **OUTPUT ATTENUATOR TEST FAILED**

An "external test 19: OUTPUT ATTENUATOR" fails. Troubleshoot the A7 output attenuator in accordance with Chapter 7.

40 **PHASE LOCK LOOP UNLOCKED**

A phase lock loop (PLL) circuits within the HP 4286A does not work properly. Troubleshoot the HP 4286A in accordance with Chapter 6 . When a **Svc** annotation is displayed (Service Modes are activated), this error message does not appear even if a PLL circuit is not working.

215 **POST REGULATOR OUTPUT VOLTAGE OUT OF SPEC**

A power supply voltage of the A2 post-regulator is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with Chapter 5.

POWER FAILED ON—-

Power failure occurs on the power lines listed in the message. One or some of +65 V, +15 V, +5 V, -5 V, -15 V, and PostRegHot, follow the message. Troubleshoot the power supply functional group in accordance with Chapter 5.

198 **POWER ON TEST FAILED**

An internal test fails in the power on sequence. This message is displayed when the power on selftest fails. Troubleshoot the HP 4286A in accordance with Chapter 4.

242 **RECEIVER GAIN OUT OF SPEC**

An "external test 23: FRONT ISOL'N" fails. A6 receiver IF gain is incorrect. Troubleshoot the receiver group in accordance with Chapter 8.

241 **RECEIVER GAIN TEST FAILED**

An "external test 20: RECEIVER GAIN" fails. Troubleshoot the receiver group in accordance with Chapter 8.

219 **REF OSC TEST FAILED**

The reference oscillator on the A5 synthesizer does not work properly. This message is displayed when an internal test 6: A5 REFERENCE OSC fails. Troubleshoot the source group in accordance with Chapter 7.

206 **RTC CHIP TEST FAILED**

The A1 CPU's RTC (Real Time Clock) does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

227 **SAMPLE FREQUENCY OUT OF SPEC**

The sampling frequency of the sample/hold circuit on the A6 receiver IF is out of its limits. This message is displayed when an internal test 13: A6 SEQUENCER fails. Troubleshoot the receiver group in accordance with Chapter 8.

228 **SOURCE LEVEL TEST FAILED**

The source level output from the A3A3 source is out of limits. This message is displayed when an "internal test 14: SOURCE LEVEL" fails. Troubleshoot the source group in accordance with Chapter 7.

232 **SOURCE FLATNESS TEST FAILED**

An "external test 18: SOURCE FLATNESS" fails. Troubleshoot the source group in accordance with Chapter 7.

226 **SOURCE OSC TEST FAILED**

The source oscillator on the A3A1 ALC does not work properly. This message is displayed when an internal test 12: A3A1 SOURCE OSC fails. Troubleshoot the source group in accordance with Chapter 7.

246 **VCXO TUNING VOLTAGE OUT OF LIMIT**

VCXO tuning voltage is incorrect, in performing an "adjustment test 28: 3RD VCXO LEVEL ADJ" or an "adjustment test 31: SOURCE VCXO LEVEL ADJ". In the 3RD VCXO LEVEL ADJ, replace the A6 receiver IF. In the SOURCE VCXO LEVEL ADJ, replace the A3A1 source vernier.

Error Messages in Numerical Order

POWER FAILED ON—-

Power failure occurs on the power lines listed in the message. One or some of +65 V, +15 V, +5 V, -5 V, -15 V, and PostRegHot, follow the message.Troubleshoot the power supply functional group in accordance with Chapter 5.

40 **PHASE LOCK LOOP UNLOCKED**

A phase lock loop (PLL) circuits within the HP 4286A does not work properly. Troubleshoot the HP 4286A in accordance with Chapter 6 . When a **Svc** annotation is displayed (Service Modes are activated), this error message does not appear even if a PLL circuit is not working.

190 **CORR. CONST. DATA LOST; DEFAULT DATA IS USED**

This message is displayed when the correction constants EEPROM data is lost and turned on in the service mode. Troubleshoot the HP 4286A in accordance with Chapter 6 .

198 **POWER ON TEST FAILED**

An internal test fails in the power on sequence. This message is displayed when the power on selftest fails. Troubleshoot the HP 4286A in accordance with Chapter 4.

199 **EEPROM WRITE ERROR**

Data cannot be stored properly into the EEPROM on the A1 CPU. This message is displayed when performing the display background adjustment or updating correction constants in the EEPROM using the adjustment program. Troubleshoot the A1 CPU in accordance with Chapter 6 .

200 **ALL INT TEST FAILED**

This message is displayed when an internal test 0: ALL INT fails. Troubleshoot the HP 4286A in accordance with Chapter 4.

201 **FLASH MEMORY CHECK SUM ERROR**

The data (Firmware) stored in the A1 flash memory are invalid. This message is displayed in the bootloader menu. Troubleshoot the A1 CPU in accordance with Chapter 6 .

202 **BACKUP SRAM CHECK SUM ERROR**

The data (HP-IB Address and so on) stored in the A1 CPU's BACKUP SRAM are invalid. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

203 **EEPROM CHECK SUM ERROR**

The data (Correction Constants and so on) stored in the A1 CPU's EEPROM are invalid. This message is displayed when an internal test 1: A1 CPU fails. Troubleshoot the A1 CPU in accordance with Chapter 6 .

204 **DSP CHIP TEST FAILED**

The A1 CPU's DSP (Digital Signal Processor) does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

205 **F-BUS TIMER CHIP TEST FAILED**

The A1 CPU's F-BUS (Frequency Bus) timer does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

206 **RTC CHIP TEST FAILED**

The A1 CPU's RTC (Real Time Clock) does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

207 **KEY CHIP TEST FAILED**

The A1 CPU's front keyboard control chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

208 **FDC CHIP TEST FAILED**

The A1 CPU's FDC (Flexible Disk drive control) ship does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

209 **HP-IB CHIP TEST FAILED**

The A1 CPU's HP-IB chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

210 **HP-HIL CHIP TEST FAILED**

The A1 CPU's HP-HIL control chip does not work properly. This message is displayed when an internal test 1: A1 CPU fails. Replace the A1 CPU with a new one. See Chapter 6 .

211 **CPU INTERNAL SRAM R/W ERROR**

The A1 CPU's internal SRAM does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See Chapter 6 .

212 **CPU BACKUP SRAM R/W ERROR**

The A1 CPU's BACKUP SRAM does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See Chapter 6 .

213 **DSP SRAM R/W ERROR**

The DSP's SRAM on the A1 CPU does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 COU with a new one. See Chapter 6 .

214 **DUAL PORT SRAM R/W ERROR**

The DSP's dual port SRAM on the A1 CPU does not work properly. This message is displayed when an internal test 2: A1 VOLATILE MEMORY fails. Replace the A1 CPU with a new one. See Chapter 6 .

215 **POST REGULATOR OUTPUT VOLTAGE OUT OF SPEC**

A power supply voltage of the A2 post-regulator is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with Chapter 5.

216 **GND LEVEL OUT OF SPEC**

The voltage of the GND (Ground) at the DC bus node 26 is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with Chapter 5.

217 **FAN POWER OUT OF SPEC**

The voltage of the fan power supply at the DC bus node 11 is out of its limits. This message is displayed when an internal test 4: A2 POST REGULATOR fails. Troubleshoot the power supply functional group in accordance with Chapter 5.

218 **FAILURE FOUND FROM A/D MUX TO A/D CONVERTER**

A trouble is found on the signal path from the A/D multiplexer to A/D converter on the A6 receiver IF. This message is displayed when an internal test 5: A6 A/D CONVERTER fails. Troubleshoot the A6 receiver IF in accordance with Chapter 8.

219 **REF OSC TEST FAILED**

The reference oscillator on the A5 synthesizer does not work properly. This message is displayed when an internal test 6: A5 REFERENCE OSC fails. Troubleshoot the source group in accordance with Chapter 7.

220 **FRACTIONAL N OSC TEST FAILED**

The fractional N oscillator on the A5 synthesizer does not work properly. This message is displayed when an internal test 7: A5 FRACTIONAL N OSC fails. Troubleshoot the source group in accordance with Chapter 7.

222 **1st LO OSC TEST FAILED**

The 1st LO OSC (first local oscillator) on the A4A1 1st LO does not work properly. This message is displayed when an internal test 8: A4A1 1ST LO OSC fails. Troubleshoot the source group in accordance with Chapter 7.

223 **2nd LO OSC TEST FAILED**

The 2nd LO OSC (second local oscillator) on the A3A2 2nd LO does not work properly. This message is displayed when an internal test 9: A3A2 2ND LO fails. Troubleshoot the source group in accordance with Chapter 7.

224 **A3 DIVIDER OUTPUT FREQUENCY OUT OF SPEC**

The output frequency of the divider circuit on the A3A1 ALC is out of its limits. This message is displayed when an internal test 10: A3A1 DIVIDER fails. Troubleshoot the source group in accordance with Chapter 7.

225 **3rd LO OSC TEST FAILED**

The 3rd LO OSC (third local oscillator) on the A6 receiver IF does not work properly. This message is displayed when an internal test 11: A6 3RD LO OSC fails. Troubleshoot the receiver group in accordance with Chapter 8.

226 **SOURCE OSC TEST FAILED**

The source oscillator on the A3A1 ALC does not work properly. This message is displayed when an internal test 12: A3A1 SOURCE OSC fails. Troubleshoot the source group in accordance with Chapter 7.

227 **SAMPLE FREQUENCY OUT OF SPEC**

The sampling frequency of the sample/hold circuit on the A6 receiver IF is out of its limits. This message is displayed when an internal test 13: A6 SEQUENCER fails. Troubleshoot the receiver group in accordance with Chapter 8.

228 **SOURCE LEVEL TEST FAILED**

The source level output from the A3A3 source is out of limits. This message is displayed when an "internal test 14: SOURCE LEVEL" fails. Troubleshoot the source group in accordance with Chapter 7.

230 **FLOPPY DISK DRIVE FAILURE FOUND**

The built-in FDD (Floppy Disk Drive) does not work properly. This message is displayed when an external test 17: DSK DR FAULT ISOL'N fails. Replace the FDD with a new one. See Chapter 6 .

232 **SOURCE FLATNESS TEST FAILED**

An "external test 19: SOURCE FLATNESS" fails. Troubleshoot the source group in accordance with Chapter 7.

233 **OUTPUT ATTENUATOR TEST FAILED**

An "external test 19: OUTPUT ATTENUATOR" fails. Troubleshoot the A7 output attenuator in accordance with Chapter 7.

239 **FRONT ISOL'N TEST FAILED**

An "external test 23: FRONT ISOL'N" fails. Troubleshoot the receiver group in accordance with Chapter 8.

241 **RECEIVER GAIN TEST FAILED**

An "external test 20: RECEIVER GAIN" fails. Troubleshoot the receiver group in accordance with Chapter 8.

242 RECEIVER GAIN OUT OF SPEC

An “external test 23: FRONT ISOL’N” fails. A6 receiver IF gain is incorrect. Troubleshoot the receiver group in accordance with Chapter 8.

243 A6 GAIN TEST FAILED

An “external test 21: A6 GAIN” fails. Replace the A6 receiver IF. See Chapter 8.

244 A6 VI NORMALIZER TEST FAILED

An “external test 22: A6 VI NORMALIZER” fails. Replace the A6 receiver IF. See Chapter 8.

245 MAX VCXO LEVEL OUT OF SPEC

Maximum VCXO level is incorrect, in performing an “adjustment test 28: 3RD VCXO LEVEL ADJ” or an “adjustment test 31: SOURCE VCXO LEVEL ADJ”. In the 3RD VCXO LEVEL ADJ, replace the A6 receiver IF. In the SOURCE VCXO LEVEL ADJ, replace the A3A1 source vernier.

246 VCXO TUNING VOLTAGE OUT OF LIMIT

VCXO tuning voltage is incorrect, in performing an “adjustment test 28: 3RD VCXOLEVEL ADJ” or an “adjustment test 31: SOURCE VCXO LEVEL ADJ”. In the 3RD VCXO LEVEL ADJ, replace the A6 receiver IF. In the SOURCE VCXO LEVEL ADJ, replace the A3A1 source vernier.